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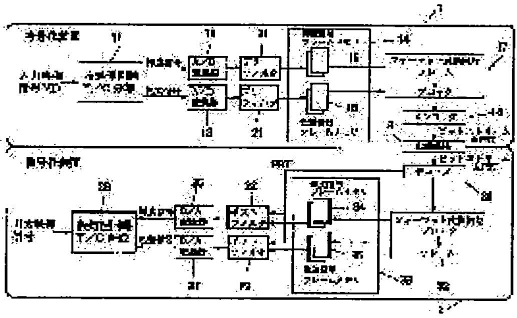
## (54) ENCODER AND DECODER FOR PICTURE SIGNAL

(57)Abstract:
PURPOSE: To best correct the decoded picture signal with a simple configuration.
CONSTITUTION: An encoder 18 of an encoding device 1 encodes a PST flag showing the encoding condition of a pre-filter 21 together with the bit stream being picture data at the same time. The bit stream and the PST flag are sent to a recording medium 3 at the same time. The bit stream and the PST flag encoded and stored in the recording medium 3 are decoded by a decoder 31 of a decoding device 2. The decoded bit stream is inputted to a format conversion circuit 32 and it is converted from the block format into the frame format. On the other hand, the decoded PST flag is sent to a post filter 22 which selects the optimal filter by the PST flag.



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## CLAIMS

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[Claim(s)]
[Claim 1]In picture signal coding equipment which it had, an encoding means which codes a picture signal based on a predetermined estimated image signal said encoding means, Picture signal coding equipment coding a coding condition flag which shows a coding condition of said picture signal when coding said picture signal based on said estimated image signal.
[Claim 2]The picture signal coding equipment according to claim 1 which said picture signal is the picture information of a bit stream, and is characterized by said coding flag existing in user area of said picture information of a bit stream.
[Claim 3]The picture signal coding equipment according to claim 2 having further a flag setting means which sets up said coding flag based on the coding bit rate of said picture information of a bit stream which said encoding means codes.
[Claim 4]In an image signal decoding device to decrypt, a coded image signal which coded a picture signal based on a predetermined estimated image signal said coded image signal, An image signal decoding device having consisted of a coding condition flag which shows a coding condition of said picture signal and said picture signal, and providing a picture compensation means which amends said decrypted picture signal based on said coding condition flag.
[Claim 5]Said picture signal is the picture information of a bit stream.
The image signal decoding device according to claim 4, wherein said coding flag exists in user area of said picture information.

[Claim 6]The image signal decoding device according to claim 5, wherein said coding flag is set up based on the coding bit rate of said picture information of a coded bit stream.
[Claim 7]An image signal decoding device of any one description of the Claims 4-6, wherein said picture compensation means consists of two or more filters, chooses said two or more

filters based on said flag and amends said picture signal.
[Claim 8]An image signal decoding device of any one description of the Claims 4-7, wherein said filter is a median filter.

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## DETAILED DESCRIPTION

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[Detailed Description of the Invention]
[0001]
[Industrial Application]This invention is used when compressing and transmitting dynamic image data, and it relates to suitable picture signal coding equipment and image signal decoding device.
[0002]
[Description of the Prior Art]When recording dynamic image data on a magneto-optical disc, magnetic tape, etc. in digital one, or when transmitting via a predetermined transmission medium, data is coded and compressed and data volume is made to decrease.
[0003]For example, like the video conference system and the video telephone system, in the system which transmits a dynamic image signal to a remote place, in order to use a transmission line efficiently, it is made as [ carry out / compression encoding of the picture signal ] using the line correlation and inter frame correlation of a video signal.
[0004]If line correlation is used, DCT (discrete cosine transform) processing can be carried out, for example, and a picture signal can be compressed.
[0005]If inter frame correlation is used, it will become possible to compress a picture signal further and to code. For example, as shown in drawing 11, when frame image PC1, PC2, and PC3 have occurred in the time t1, t2, and t3, respectively, The difference of the picture signal of the frame images PC1 and PC2 is calculated, PC12 is generated, and the difference of the frame images PC2 and PC3 is calculated, and PC23 is generated. Usually, since the picture of the frame which adjoins in time does not have a so big change, if both difference is calculated, the differential signal will become a thing of a small value. Then, a code amount is compressible if this differential signal is coded.
[0006]However, the original picture cannot be restored if only the differential signal was transmitted. Then, the picture of each frame is made into one picture of three kinds of pictures,

I picture, P picture, or B picture, and it is made to carry out compression encoding of the picture signal.

[0007]That is, as shown, for example in drawing 12, frame F1 thru/or the picture signal of 17 frames to F17 are made into a glue PUOBU picture (GOP), and it may be one unit of processing. And the picture signal of frame F1 of the head is coded as an I picture, and the 2nd frame F2 processes the 3rd frame F3 as a B picture as a P picture, respectively. Hereafter, the frames F4 thru/or F17 of the 4th henceforth are processed by turns as B picture or a P picture.

[0008]As a picture signal of I picture, the picture signal for the one frame is transmitted as it is. On the other hand, as a picture signal of P picture, fundamentally, as shown in drawing 12 (A), the difference from the picture signal of I picture or P picture preceded in time than it is transmitted. Furthermore, as a picture signal of B picture, fundamentally, as shown in drawing 12 (B), it asks for the difference from the average value of both the frame preceded in time or the frame which carries out backward, and the difference is coded.

[0009]Drawing 13 is carried out in this way, and the principle of the method of coding a dynamic image signal is shown. As shown in the figure, since the first frame F1 is processed as an I picture, it is transmitted to a transmission line as transmission data F1X as it is (formation of a picture inner code). On the other hand, since the 2nd frame F2 is processed as a B picture, the difference (prediction error) of frame F1 preceded in time and the average value of the frame F3 which carries out backward in time calculates, and the difference is transmitted as the transmission data F2X.

[0010]However, if the processing as this B picture is explained still more finely, they exist. [ four kinds of ] The 1st processing transmits the data of the original frame F2 as the transmission data F2X as it is, and turns into the same processing as the case in I picture (SP1) (intra (prediction within a picture) coding). The 2nd processing calculates the difference from the next frame F3 in time, and transmits the difference (SP2) (backward prediction coding). The 3rd processing transmits difference (SP3) with frame F1 preceded in time (forward prediction coding). Furthermore, the 4th processing generates difference (SP4) with the average value of the frame F3 which carries out backward to frame F1 preceded in time, and transmits this as the transmission data F2X (both-directions prediction coding).

[0011]The way transmission data decreases most among these four methods is adopted.

[0012]The motion vector x1 (frame F1 and motion vector between F2) (in the case of forward prediction) between the pictures (estimated image) of the frame which serves as an object which calculates difference when transmitting difference data, Or both x2 (motion vector between the frames F3 and F2) (in the case of backward prediction), or x1 and x2 (in the case of both-directions prediction) are transmitted with difference data.

[0013]A differential signal (SP3) with this frame and the motion vector x3 calculate the frame

F3 of P picture by using as an estimated image frame F1 preceded in time, and this is transmitted as the transmission data F3X (forward prediction coding). Or the data of the original frame F3 is transmitted as the data F3X as it is again (intra coding). (SP1) As for whether it is transmitted by which method, the direction whose transmission data decreases more is chosen like the case in B picture.

[0014]Drawing 14 codes and transmits a dynamic image signal based on the principle mentioned above, and the example of composition of the device which decrypts this is shown. The coding equipment 1 codes the inputted video signal, and is made as [ transmit / to the recording medium 3 as a transmission line ]. And the decoding device 2 reproduces the signal recorded on the recording medium 3, and is made as [ output / this / decode and ].

[0015]In the coding equipment 1, the inputted video signal is inputted into the preprocessing circuit 11, a luminance signal and a chrominance signal (in the case of this working example color-difference signal) are separated there, and an A/D conversion is carried out with A/D converters 12 and 13, respectively. The video signal which the A/D conversion was carried out with A/D converters 12 and 13, and turned into a digital signal is supplied to the back frame memory 14 processed by the pre-filter 21, and is memorized. The frame memory 14 memorizes a luminance signal to the luminance-signal frame memory 15, and makes the color-difference-signal frame memory 16 memorize a color-difference signal, respectively.

[0016]The pre-filter 21 performs processing for raising encoding efficiency. This is for example, a noise rejection filter, and is a filter for restricting a zone.

[0017]The format conversion circuit 17 changes into the signal of a block format the signal of the frame format memorized by the frame memory 14. That is, as shown in drawing 15, let the video signal memorized by the frame memory 14 be the data of a frame format in which the lines of V lines of H dot were collected per line. The format conversion circuit 17 classifies this signal of one frame into N slices by making 16 lines into a unit. And each slice is divided into M macro blocks. Each macro block is constituted by the luminance signal corresponding to 16x16 pixels (dot), and this luminance signal is classified into block Y [1] which makes further 8x8 dots a unit thru/or Y [4]. And the Cb signal of 8x8 dots and the Cr signal of 8x8 dots are equivalent to this luminance signal of 16x16 dots.

[0018]Thus, the data changed into the block format is supplied to the encoder 18 from the format conversion circuit 17, and encoding (coding) is performed here. The details are later mentioned with reference to drawing 16.

[0019]The signal encoded by the encoder 18 is outputted to a transmission line as a bit stream. For example, the record circuit 19 is supplied and it is recorded on the recording medium 3 as a digital signal.

[0020]The data reproduced by the regenerative circuit 30 from the recording medium 3 is supplied to the decoder 31 of the decoding device 2, and is decoded. The details of the decoder 31 are later mentioned with reference to drawing 19.

[0021]The data decoded by the decoder 31 is inputted into the format conversion circuit 32, and is changed into a frame format from a block format. And the luminance signal of a frame format is supplied to the luminance-signal frame memory 34 of the frame memory 33, and is memorized, and a color-difference signal is supplied to the color-difference-signal frame memory 35, and is memorized. After being processed by the postfilter 22, D/A conversion of the luminance signal and color-difference signal which were read from the luminance-signal frame memory 34 and the color-difference-signal frame memory 35 is carried out by D/A converters 36 and 37, respectively, and they are supplied to the post-processing circuit 38, and are compounded. And for example, it is outputted and displayed on the display of CRT etc. which are not illustrated.

[0022]The postfilter 22 performs processing for improving image quality. For example, it is a filter for removing block distortion and a mosquito noise.

[0023]Next, the example of composition of the encoder 18 is explained with reference to drawing 16.

[0024]The image data which should be coded is inputted into the motion vector detection circuit 50 by a macro block unit. The motion vector detection circuit 50 processes the image data of each frame as I picture, P picture, or a B picture according to the predetermined sequence set up beforehand. Whether the picture of each frame inputted sequentially is processed as which picture of I, P, and B. it is set beforehand (for example, the glue PUOBU picture constituted by frame F1 thru/or F17 as shown in drawing 15 -- I, B, P, B, P, and ... processed as B and P).

[0025]The image data of the frame (for example, frame F1) processed as an I picture, The image data of the frame (for example, frame F2) which is transmitted and memorized by the front original image part 51a of the frame memory 51 from the motion vector detection circuit 50, and is processed as a B picture, The reference original image part 51b transmits and memorizes, and the image data of the frame (for example, frame F3) processed as a P picture is transmitted and memorized by the back original image part 51c.

[0026]When the picture of the frame which should be further processed as B picture (frame F4) or a P picture (frame F5) is inputted in the following timing, The image data of the first P picture (frame F3) memorized by the back original image part 51c till then, It is transmitted to the front original image part 51a, the image data of the following B picture (frame F4) is memorized by the reference original image part 51b (overwrite), and the image data of the following P picture (frame F5) is memorized by the back original image part 51c (overwrite). Such operation is repeated successively.

[0027]The signal of each picture memorized by the frame memory 51 is read from there, and frame prediction mode processing or field prediction mode processing is performed in the prediction mode switching circuit 52. In the operation part 53, the operation of the prediction within a picture, forward prediction, backward prediction, or both-directions prediction is performed under control of the prediction decision circuit 54 further again. It is determined corresponding to a prediction error signal (difference of the image comparison made into the object of processing, and the estimated image to this) whether to perform processing [ which ] among these processings. For this reason, the motion vector detection circuit 50 generates the absolute value sum (the sum of squares may be sufficient) of the prediction error signal used for this judgment.

[0028]Here, the frame prediction mode and field prediction mode in the prediction mode switching circuit 52 are explained.

[0029]When frame prediction mode is set up, the prediction mode switching circuit 52 outputs four luminosity block Y [1] supplied from the motion vector detection circuit 50 thru/or Y [4] to the latter operation part 53 as it is. Namely, it is in the state where the data of the line of an odd number field and the data of the line of an even number field were intermingled in each luminosity block, as [ show / in drawing 8 ] in this case. In this frame prediction mode, prediction is performed by making four luminosity blocks (macro block) into a unit, and one motion vector corresponds to four luminosity blocks.

[0030]On the other hand, the prediction mode switching circuit 52, As shown in drawing 17 (B), the signal inputted from the motion vector detection circuit 50 in field prediction mode with the composition shown in drawing 17 (A), Accept luminosity block Y [1] and Y [2], for example by the dot of the line of an odd number field, and they are made to constitute among four luminosity blocks, the data of the line of an even number field is made to constitute other two luminosity block Y [3] and Y [4], and they are outputted to the operation part 53. In this case, one motion vector corresponds to two luminosity block Y [1] and Y [2], and other one motion vector corresponds to other two luminosity block Y [3] and Y [4].

[0031]The motion vector detection circuit 50 outputs the absolute value sum of the prediction error in frame prediction mode, and the absolute value sum of the prediction error in field prediction mode to the prediction mode switching circuit 52. The prediction mode switching circuit 52 compares the absolute value sum of the prediction error in frame prediction mode and field prediction mode, performs processing corresponding to the prediction mode in which the value is small, and outputs data to the operation part 53.

[0032]However, such processing is performed actually in the motion vector detection circuit 50. That is, the motion vector detection circuit 50 outputs the signal of the composition corresponding to the determined mode to the prediction mode switching circuit 52, and the prediction mode switching circuit 52 outputs the signal to the latter operation part 53 as it is.

[0033]In the case of frame prediction mode, as shown in drawing 17 (A), a color-difference signal is in the state where the data of the line of an odd number field and the data of the line of an even number field are intermingled, and is supplied to the operation part 53. In the case of field prediction mode, as shown in drawing 17 (B), each color difference block Cb and the upper half (four lines) of Cr, It is considered as the color-difference signal of the odd number field corresponding to luminosity block Y [1] and Y [2], and a lower half (four lines) is made into the color-difference signal of the even number field corresponding to luminosity block Y [3] and Y [4].

[0034]The motion vector detection circuit 50 generates [ in / as follows / the prediction decision circuit 54 ] the absolute value sum of the prediction error for determining whether to perform prediction [ which / of the prediction within a picture, forward prediction, backward prediction, or both-directions prediction ].

[0035]That is, the difference of peace sigma|Aij | of absolute value |sigmaAij| of peace sigmaAij of the signal Aij of the macro block of an image comparison and absolute value |Aij| of the signal Aij of a macro block is searched for as an absolute value sum of the prediction error of the prediction within a picture. It asks for peace sigma|Aij-Bij [ of absolute value |Aij-Bij| of difference Aij-Bij of the signal Aij of the macro block of an image comparison, and the signal Bij of the macro block of an estimated image ] | as an absolute value sum of the prediction error of forward prediction. It asks for the absolute value sum of the prediction error of backward prediction and both-directions prediction as well as (changing the estimated image into a different estimated image from the case in forward prediction) the case in forward prediction.

[0036]These absolute value sums are supplied to the prediction decision circuit 54. The prediction decision circuit 54 chooses the smallest thing as an absolute value sum of the prediction error of the Inta prediction among the absolute value sums of the prediction error of forward prediction, backward prediction, and both-directions prediction. The absolute value sum of the prediction error of this Inta prediction is compared with the absolute value sum of the prediction error of the prediction within a picture, the smaller one of it is chosen, and the mode corresponding to this selected absolute value sum is chosen as prediction mode. That is, if the absolute value sum of the prediction error of the prediction within a picture is smaller, the prediction mode within a picture will be set up. If the absolute value sum of the prediction error of the Inta prediction is smaller, the mode whose absolute value sum corresponding among forward prediction, backward prediction, or both-directions prediction mode was the smallest will be set up.

[0037]Thus, the motion vector detection circuit 50 is the composition corresponding to the mode chosen by the prediction mode switching circuit 52 among a frame or field prediction mode in the signal of the macro block of an image comparison, While supplying the operation part 53 via the prediction mode switching circuit 52, the motion vector between the estimated image corresponding to the prediction mode in which the prediction decision circuit 54 was selected among four prediction modes, and an image comparison is detected, and it outputs to the variable-length-coding circuit 58 and the motion compensation circuit 65. As mentioned above, that from which the corresponding absolute value sum of a prediction error serves as the minimum as this motion vector is chosen.

[0038]When the motion vector detection circuit 50 has read the image data of I picture from the front original image part 51a in the prediction decision circuit 54, As prediction mode, a frame or field (picture) inner prediction mode (mode in which a motion compensation is not performed) is set up, and the switch 53d of the operation part 53 is changed to the point-of-contact a side. Thereby, the image data of I picture is inputted into the DCT mode switching circuit 55.

[0039]As shown in drawing 18 (A) or drawing 18 (B), this DCT mode switching circuit 55, The data of four luminosity blocks is changed into the state (frame DCT mode) where the line of an odd number field and the line of an even number field are intermingled or the separated state (field DCT mode), and the state of ********, and is outputted to DCT circuit 56.

[0040]That is, the DCT mode switching circuit 55 compares the encoding efficiency at the time of being intermingled and carrying out DCT processing of the data of an odd number field and an even number field with the encoding efficiency at the time of carrying out DCT processing in the state where it dissociated, and chooses the mode with good encoding efficiency.

[0041]For example, the inputted signal is considered as the composition in which the line of an odd number field and an even number field is intermingled as shown in drawing 18 (A), the difference of the signal of the line of an odd number field and the signal of the line of an even number field which adjoins up and down is calculated, and it asks for the sum (or sum of squares) of the absolute value further. The difference of the signal of the lines of the odd number field which considers the inputted signal as the composition which the line of an odd number field and an even number field separated as shown in drawing 18 (B), and adjoins up and down, The difference of the signal of the lines of an even number field is calculated, and it asks for the sum (or sum of squares) of each absolute value. Both (absolute value sum) are compared and the DCT mode corresponding to a small value is set up. That is, if former one is small, frame DCT mode will be set up, and if latter one is small, field DCT mode will be set up.

[0042]And while outputting the data of the composition corresponding to the selected DCT mode to DCT circuit 56, the DCT flag which shows the selected DCT mode is outputted to the variable-length-coding circuit 58, the DCT-blocks rearrangement circuit 62, and the motion compensation circuit 65.

[0043]The prediction mode (drawing 17) in the prediction mode switching circuit 52 is compared with the DCT mode (drawing 18) in this DCT mode switching circuit 55, and the data structure [ in / about a luminosity block / each mode of both ] is substantially the same so that clearly.

[0044]Also in [ when frame prediction mode (mode in which an odd line and an even line are intermingled) is chosen in the prediction mode switching circuit 52 ] the DCT mode switching circuit 55, In [ a possibility that frame DCT mode (mode in which an odd line and an even line are intermingled) will be chosen is high, and ] the prediction mode switching circuit 52, When field prediction mode (mode in which the data of an odd number field and an even number field was separated) is chosen, in the DCT mode switching circuit 55, a possibility that field DCT mode (mode in which the data of an odd number field and an even number field was separated) will be chosen is high.

[0045]However, it not necessarily always is not necessarily made such, the mode is determined that the absolute value sum of a prediction error will become small in the prediction mode switching circuit 52, and the mode is determined that encoding efficiency will become good in the DCT mode switching circuit 55.

[0046]It is inputted into DCT circuit 56, DCT (discrete cosine transform) processing is carried out, and the image data of I picture outputted from the DCT mode switching circuit 55 is changed into a DCT coefficient. This DCT coefficient is inputted into the variable-length-coding circuit 58, after being inputted into the quantization circuit 57 and quantized by the quantization step corresponding to the data accumulation amount (buffer accumulated dose) of the transmission buffer 59.

[0047]Corresponding to the quantization step (scale) supplied from the quantization circuit 57, the image data (in the case of now data of I picture) supplied from the quantization circuit 57 is changed into variable length codes, such as Huffman coding, for example, and the variable-length-coding circuit 58 outputs it to the transmission buffer 59.

[0048]In the variable-length-coding circuit 58, from the quantization circuit 57 again A quantization step (scale), the prediction decision circuit 54 -- prediction mode (the prediction within a picture, forward prediction, and backward prediction.) Any of both-directions prediction were set up from the mode and the motion vector detection circuit 50 which are shown Or a motion vector, From the prediction mode switching circuit 52, a prediction flag (flag which shows any should be set up between frame prediction mode or field prediction mode), And the DCT flag (flag which shows any should be set up between frame DCT mode or field DCT mode) which the DCT mode switching circuit 55 outputs is inputted, and variable length coding also of these is carried out.

[0049]The transmission buffer 59 stores the inputted data temporarily, and outputs the data corresponding to an accumulated dose to the quantization circuit 57. The transmission buffer 59 will reduce the data volume of quantization data by enlarging the quantizing scale of the quantization circuit 57 with a quantized control signal, if the data residue increases to permission upper limit. Contrary to this, if a data residue decreases to a permission lower limit, the transmission buffer 59 will increase the data volume of quantization data by making the quantizing scale of the quantization circuit 57 small with a quantized control signal. Thus, overflow or underflow of the transmission buffer 59 is prevented.

[0050]And the data stored in the transmission buffer 59 is read to predetermined timing, and is outputted to a transmission line, for example, is recorded on the recording medium 3.

[0051]On the other hand, the data of I picture outputted from the quantization circuit 57 is inputted into the inverse quantizing circuit 60, and inverse quantization is carried out corresponding to the quantization step supplied from the quantization circuit 57. The output of the inverse quantizing circuit 60 is inputted into the IDCT (reverse DCT) circuit 61, and after reverse DCT processing is carried out, it is inputted into the DCT-blocks rearrangement circuit 62. The DCT-blocks rearrangement circuit 62 performs a data list substitute corresponding to the prediction flag to which the inputted data is supplied from the prediction mode switching circuit 52, and the DCT flag supplied from the DCT mode switching circuit 55.

[0052]Namely, in the prediction mode switching circuit 52, when frame prediction mode is set up, it is in the state where the data of an odd number field and the data of an even number field are intermingled the data which is read from the motion compensation circuit 65 and supplied to the operation part 53. This data is supplied also to the computing unit 63. For this reason, the DCT-blocks rearrangement circuit 62, When frame DCT mode is set up in the data supplied from the IDCT circuit 61, Since it is in the state where the data of an odd number field and the data of the even number field were separated when the computing unit 63 is then supplied and field DCT mode is set up, data is rearranged into the state where these are intermingled and it outputs to the computing unit 63.

[0053]On the other hand, in the prediction mode switching circuit 52, when field prediction mode is set up, it is in the state where the data of an odd number field and the data of the even number field dissociated the data supplied to the operation part 53 from the motion compensation circuit 65. For this reason, the DCT-blocks rearrangement circuit 58 supplies the data outputted from the IDCT circuit 61 to the computing unit 63 as it is, when field DCT mode is set up by the DCT mode switching circuit 55, but. Since it is in the state where the data of an odd number field and the data of an even number field are intermingled when frame DCT mode is set up, each rearranges this into the state where it dissociated, and outputs it to the computing unit 63.

[0054]That is, the DCT-blocks rearrangement circuit 58 performs the data list substitute which the IDCT circuit 61 outputs so that it may be from the motion compensation circuit 65 in the same array state as the array state of the data supplied to the operation part 53.

[0055]Since the data which is outputted from the IDCT circuit 61 in now is data of I picture, it is considered as the prediction within a picture. For this reason, while the DCT mode switching circuit 55 is outputting the frame DCT flag, as it is, via the computing unit 63, the data outputted from the IDCT circuit 61 is supplied to the forward prediction picture part 65a of the frame memory 65, and is memorized. It memorizes, after a data list substitute is performed, when the field DCT flag is outputted.

[0056]The motion vector detection circuit 50 the image data of each frame inputted sequentially, For example, I, B, P, B, P, B ... When processing as a picture, respectively, After processing the image data of the frame inputted first as an I picture, before processing the picture of the frame inputted into the next as a B picture, the image data of the frame further inputted into the next is processed as a P picture. It is because it cannot decode unless P picture as a backward prediction image is prepared previously, in order to accompany B picture by backward prediction.

[0057]Then, the motion vector detection circuit 50 is processing of I picture, next starts processing of the image data of P picture memorized by the back original image part 51c. And the absolute value sum of the inter-frame difference (prediction error) in a macro block unit is supplied to the prediction mode switching circuit 52 and the prediction decision circuit 54 from the motion vector detection circuit 50 like the case where it mentions above. The prediction mode switching circuit 52 and the prediction decision circuit 54 set up the prediction mode of a frame / field prediction mode or the prediction within a picture, forward prediction, backward prediction, or both-directions prediction corresponding to the absolute value sum of the prediction error of the macro block of this P picture.

[0058]When the prediction mode within a picture is set up, the operation part 53 is changed to the point-of-contact a side, as the switch 53d was mentioned above. Therefore, this data is transmitted to a transmission line like the data of I picture via the DCT mode switching circuit 55, DCT circuit 56, the quantization circuit 57, the variable-length-coding circuit 58, and the transmission buffer 59. Via the inverse quantizing circuit 60, the IDCT circuit 61, the DCT-blocks rearrangement circuit 62, and the computing unit 63, this data is supplied to the backward prediction picture part 64b of the frame memory 64, and is memorized.

[0059]While the switch 53d is changed to the point of contact b at the time of forward prediction mode, The picture (in case of now picture of I picture) data memorized by the forward prediction picture part 64a of the frame memory 64 is read, and a motion compensation is carried out by the motion compensation circuit 65 corresponding to the motion vector which the motion vector detection circuit 50 outputs. Namely, when it is ordered the motion compensation circuit 65 in setting out in forward prediction mode from the prediction decision circuit 54, Only the part corresponding to the position lost-motion vector corresponding to the position of the macro block to which the motion vector detection circuit 50 is outputting the reading address of the forward prediction picture part 64a now is shifted, data is read, and prediction image data is generated.

[0060]The prediction image data outputted from the motion compensation circuit 65 is supplied to the computing unit 53a. The computing unit 53a subtracts the prediction image data corresponding to this macro block supplied from the motion compensation circuit 65 from the data of the macro block of the image comparison supplied from the prediction mode switching circuit 52, and outputs that difference (prediction error). This difference data is transmitted to a transmission line via the DCT mode switching circuit 55, DCT circuit 56, the quantization circuit 57, the variable-length-coding circuit 58, and the transmission buffer 59. This difference data is locally decoded by the inverse quantizing circuit 60, the IDCT circuit 61, and the DCT-blocks rearrangement circuit 62, and is inputted into the computing unit 63.

[0061]The same data as the prediction image data currently supplied to the computing unit 53a is supplied to this computing unit 63 again. The computing unit 63 adds the prediction image data which the motion compensation circuit 65 outputs to the difference data which the DCT-blocks rearrangement circuit 62 outputs. Thereby, the image data of the original P (it decoded) picture is obtained. The image data of this P picture is supplied to the backward prediction picture part 64b of the frame memory 64, and is memorized.

[0062]In this way, the motion vector detection circuit 50 performs processing of B picture next, after the data of I picture and P picture is memorized by the forward prediction picture part 64a and the backward prediction picture part 64b, respectively. The prediction mode switching circuit 52 and the prediction decision circuit 54, Corresponding to the size of the absolute value sum of the inter-frame difference in a macro block unit, a frame/field mode is set up and prediction mode is set to either the prediction mode within a picture, forward prediction mode, backward prediction mode or both-directions prediction mode.

[0063]As mentioned above, the switch 53d is changed to the point of contact a or b at the time of the prediction mode within a picture, or forward prediction mode. At this time, the same processing as the case in P picture is performed, and data is transmitted.

[0064]On the other hand, when backward prediction mode or both-directions prediction mode is set up, the switch 53d is changed to the point of contact c or d, respectively.

[0065]It is read by the picture (in case of now picture of P picture) data memorized by the backward prediction picture part 64b at the time of the backward prediction mode in which the switch 53d is changed to the point of contact c, and by the motion compensation circuit 65. A motion compensation is carried out corresponding to the motion vector which the motion vector detection circuit 50 outputs. Namely, when it is ordered the motion compensation circuit 65 in setting out in backward prediction mode from the prediction decision circuit 54, Only the part corresponding to the position lost-motion vector corresponding to the position of the macro block to which the motion vector detection circuit 50 is outputting the reading address of the backward prediction picture part 64b now is shifted, data is read, and prediction image data is generated.

[0066]The prediction image data outputted from the motion compensation circuit 65 is supplied to the computing unit 53b. The computing unit 53b subtracts the prediction image data supplied from the motion compensation circuit 65 from the data of the macro block of the image comparison supplied from the prediction mode switching circuit 52, and outputs the difference. This difference data is transmitted to a transmission line via the DCT mode switching circuit 55, DCT circuit 56, the quantization circuit 57, the variable-length-coding circuit 58, and the transmission buffer 59.

[0067]The picture (in case of now picture of I picture) data memorized by the forward prediction picture part 64a at the time of the both-directions prediction mode in which the switch 53d is changed to the point of contact d, The picture (in case of now picture of P picture) data memorized by the backward prediction picture part 64b is read, and a motion compensation is carried out by the motion compensation circuit 65 corresponding to the motion vector which the motion vector detection circuit 50 outputs. Namely, when it is ordered the motion compensation circuit 65 in setting out in both-directions prediction mode from the prediction decision circuit 54, The reading address of the forward prediction picture part 64a and the backward prediction picture part 64b, The motion vector detection circuit 50 shifts only the part corresponding to the position lost-motion vector (the motion vector in this case is set to two, the object for forward prediction pictures, and the object for backward prediction pictures) corresponding to the position of the macro block outputted now, reads data, and generates prediction image data.

[0068]The prediction image data outputted from the motion compensation circuit 65 is supplied to the computing unit 53c. The computing unit 53c subtracts the average value of the prediction image data supplied from the motion compensation circuit 65 from the data of the macro block of the image comparison supplied from the motion vector detection circuit 50, and outputs the difference. This difference data is transmitted to a transmission line via the DCT mode switching circuit 55, DCT circuit 56, the quantization circuit 57, the variable-length-coding circuit 58, and the transmission buffer 59.

[0069]Since the picture of B picture is not used as the estimated image of other pictures, it is not memorized by the frame memory 64.

[0070]In the frame memory 64, bank switching is performed if needed, and to a predetermined image comparison, the forward prediction picture part 64a and the backward prediction picture part 64b can change what is memorized on one side or another side as a forward prediction picture or a backward prediction picture, and can output it.

[0071]Although explained above focusing on the luminosity block, also about a color difference block, it is processed as a unit and the macro block shown in drawing 15 and the same macro block are transmitted. What set to one half the motion vector of the luminosity block with which the motion vector in the case of processing a color difference block corresponds to the perpendicular direction and the horizontal direction, respectively is used.

[0072]Drawing 19 is a block diagram showing the composition of the decoder circuit 90 which is one working example of the decoder 31 of drawing 14. After being received in the receiving circuit which is not illustrated, or being reproduced in a regenerative circuit and storing temporarily the coded image data which was transmitted via the transmission line (recording medium 3) at the receive buffer 81, it is supplied to the variable length decoding circuit 82 of the decoder circuit 90. The variable length decoding circuit 82 carries out variable-length decryption of the data supplied from the receive buffer 81, While outputting a motion vector, prediction mode, a prediction flag, and a DCT flag to the motion compensation circuit 88 and outputting a quantization step (scale) to the inverse quantizing circuit 83, respectively, the decoded image data is outputted to the inverse quantizing circuit 83. A DCT flag and a prediction flag are outputted to the inverse quantizing circuit 83.

[0073]The inverse quantizing circuit 83 carries out inverse quantization of the image data supplied from the variable length decoding circuit 82 according to the quantization step similarly supplied from the variable length decoding circuit 82, and outputs it to the IDCT circuit 84. The data (DCT coefficient) outputted from the inverse quantizing circuit 83 is the IDCT circuit 84, and reverse DCT processing is carried out and it is returned to the original image data.

[0074]This image data is further inputted into the DCT-blocks rearrangement circuit 86. Corresponding to a DCT flag and a prediction flag, the DCT-blocks rearrangement circuit 86 rearranges so that it may be in the same array state as the data which the motion compensation circuit 88 outputs to the operation part 87, and it outputs this data to the computing unit 87.

[0075]When the image data supplied from the DCT-blocks rearrangement circuit 86 is data of I picture, The data is outputted from the computing unit 86, for prediction-image-data generation of the image data (data of P picture or B picture) behind inputted into the computing unit 86, is supplied to the forward prediction picture part 87a of the frame memory 87, and is memorized. This data is outputted to the format conversion circuit 32 (drawing 14).

[0076]The image data supplied from the IDCT circuit 84 is data of P picture which uses the image data in front of one of them as prediction image data, When it is data in forward prediction mode, the image data (data of I picture) before [ one ] the forward prediction picture part 87a of the frame memory 87 memorizes is read, and the motion compensation corresponding to the motion vector outputted from the variable length decoding circuit 82 in the motion compensation circuit 88 is given. And in the computing unit 86, it is added with the image data (data of difference) supplied from the DCT-blocks rearrangement circuit 86, and is outputted. For prediction-image-data generation of the image data (data of B picture or P picture) behind inputted into the computing unit 86, this added data, i.e., the decoded data of P picture, is supplied to the backward prediction image part 87b of the frame memory 87, and it is memorized.

[0077]Even if it is data of P picture, as for the data in the prediction mode within a picture, like the data of I picture, the computing unit 87 does not perform processing in particular, but the backward prediction picture part 87b memorizes as it is.

[0078]Since this P picture is a picture which should be displayed on the next of the following B picture, it is not outputted to the format conversion circuit 32 yet at this time (as mentioned above, P picture inputted after B picture is processed ahead of B picture, and is transmitted).

[0079]When the image data supplied from the DCT-blocks rearrangement circuit 86 is data of B picture, it corresponds to the prediction mode supplied from the variable length decoding circuit 82, The image data of I picture memorized by the forward prediction picture part 87a of the frame memory 87 (in the case of forward prediction mode), The image data of P picture memorized by the backward prediction picture part 87b (in the case of backward prediction mode), Or the image data (in the case of both-directions prediction mode) of the both is read, the motion compensation corresponding to the motion vector outputted from the variable length decoding circuit 82 is given in the motion compensation circuit 88, and an estimated image is generated. However, an estimated image is not generated when you do not need a motion compensation (in the case of the prediction mode within a picture).

[0080]Thus, the data in which the motion compensation was given is added with DCT-blocks rearrangement circuit 86 output in the computing unit 86 in the motion compensation circuit 88. This added output is outputted to the format conversion circuit 32.

[0081]However, this added output is data of B picture, and since it is not used for estimated image generation of other pictures, it is not memorized by the frame memory 87.

[0082]After the picture of B picture is outputted, the image data of P picture memorized by the backward prediction picture part 87b is read, and the format conversion circuit 32 is supplied via the motion compensation circuit 88 and the computing unit 86. However, a motion compensation is not performed at this time.

[0083]Although the circuit corresponding to the prediction mode switching circuit 52 and the DCT mode switching circuit 55 in the encoder 18 of drawing 16 is not illustrated by this decoder 31, The motion compensation circuit 88 performs processing which returns the processing corresponding to these circuits, i.e., the composition from which the signal of the line of an odd number field and an even number field was separated, to the intermingled original composition if needed.

[0084]Although processing of the luminance signal was explained above, it is similarly carried out about the treatment of a color-difference signal. However, that to which the motion vector set the thing for luminance signals to one half to the perpendicular direction and the horizontal direction is used.

[0085]

[Problem(s) to be Solved by the Invention]When it has the postfilter 22 like the decoding device shown in drawing 14, various kinds of filters exist in the postfilter 22, but it is dependent on the character of image quality, and the conditions at the time of coding what kind of filter is the optimal.

[0086]For example, since degradation of the decrypted picture is remarkable when the coding bit rate is low, in order to compensate this, it is necessary to cover the filter for improving image quality strongly. On the other hand, when the coding bit rate is high, the decrypted picture remains as it is, high definition is maintained and the same filter as the case of a low bit rate is used, there is a problem of making image quality deteriorate by that cause.

[0087]A pacey picture has bad encoding efficiency, for example, considering only the case of a low bit rate, since degradation becomes remarkable at image quality, it is necessary to cover the filter for improving image quality strongly but, and when this is used for a picture with sufficient encoding efficiency, there is a problem of worsening image quality on the contrary.

[0088]That is, there is a problem that the conventional image data can be compressed and image data cannot be elongated the optimal corresponding to the character of image quality or the conditions at the time of coding with numerals and the image signal processor to decrypt.

[0089]In light of the above-mentioned circumstances, this invention is a thing.
The purpose is to provide the picture signal coding equipment and the image signal decoding device which can amend the picture signal which was boiled and was decrypted more the optimal.

[0090]

[Means for Solving the Problem]In picture signal coding equipment with which the picture signal coding equipment according to claim 1 was provided with the encoder 18 as an encoding means which codes a picture signal based on a predetermined estimated image signal, When coding a picture signal based on an estimated image signal, the encoder 18 is constituted so that a coding condition flag which shows a coding condition of a picture signal may be coded.

[0091]The picture signal coding equipment according to claim 1 makes a picture signal picture information of a bit stream, A coding flag is made to exist in user area of said picture information of a bit stream, and it can have the postfilter selection circuitry 140 as a flag setting means which sets up a coding flag based on the coding bit rate of picture information of a bit stream which the encoder 18 codes.

[0092]In an image signal decoding device to decrypt, an image signal decoding device of Claim 4 a coded image signal which coded a picture signal based on a predetermined estimated image signal a coded image signal, It consists of a coding condition flag which shows a coding condition of a picture signal and a picture signal, and based on a coding condition flag, the postfilter 22 as a picture compensation means which amends a decrypted picture signal is provided, and it is constituted.

[0093]

[work --] for By coding a coding condition flag which shows a coding condition of a picture signal in the picture signal coding equipment according to claim 1, when coding a picture signal based on an estimated image signal with the encoder 18. It makes it possible to amend a picture signal the optimal by easy composition, based on a coding condition flag, when decoding a picture signal.

[0094]In the picture signal coding equipment according to claim 1, it makes it possible to amend a picture signal to optimum more by setting up a coding flag based on the coding bit rate of picture information of a bit stream which the encoder 18 codes by the postfilter selection circuitry 140.

[0095]By amending a picture signal decrypted in an image signal decoding device of Claim 4 based on a coding condition flag which shows a coding condition of a picture signal by the postfilter 22. It makes it possible to amend a picture signal the optimal by easy composition, based on a coding condition flag, when decoding a picture signal.

[0096]

[Example]Since the 1st working example of drawing 1 has the same composition as a conventional example, only different composition is explained, the same numerals are attached to an identical configuration, and explanation is omitted.

[0097]The image data coding equipment 1 and the image data decoding device 2 of the 1st working example, As the composition of the encoder 18, the decoder 31, and the postfilter 22 differs from a conventional example and it is shown in drawing 1, in this example the encoder 18 of the coding equipment 1, Simultaneously with the bit stream which is image data, the PST flag which shows the coding condition of the pre-filter 21 is coded, and a PST flag is transmitted to the recording medium 3 with a bit stream.

[0098]The bit stream and PST flag which were coded by the recording medium 3 and memorized are decrypted by the decoder 31 of the decoding device 2, and the decrypted bit stream is inputted into the format conversion circuit 32, and is changed into a frame format from a block format. On the other hand, the decrypted PST flag is transmitted to the postfilter 22, and chooses an optimum filter with a PST flag in the postfilter 22.

[0099]The determination of the PST flag by the encoder 18 is made by a method as shown below by this example. That is, it is the method of inputting and setting up a PST flag compulsorily from the outside, and the deciding method of this PST flag is explained.

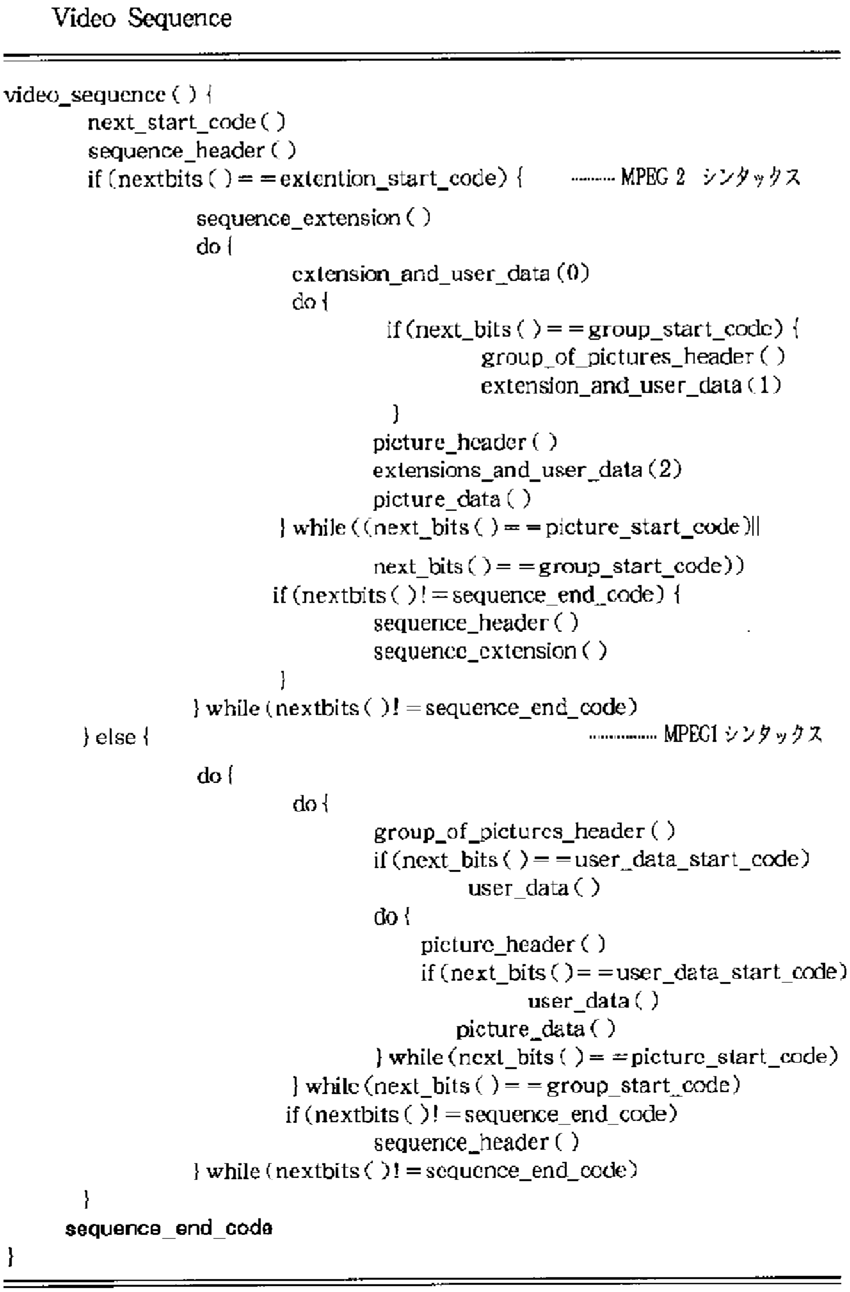
[0100]The composition of the encoder 18 which realizes this deciding method is shown in drawing 2. The inputted PST flag is inputted into the variable-length-coding circuit 58. And in the variable-length-coding circuit 58, variable length coding of the bit stream is carried out like a conventional example, and variable length coding of the inputted PST flag is carried out.

[0101]And a PST flag is memorized by the storage 3 with a bit stream as the user datum (user data) in a bit stream. In MPEG and an MPEG2 system, since "user data" can be set up after a sequence, GOP, and a picture header, a PST flag can be similarly set up per a sequence, GOP, and picture header.

[0102]Here, the syntax of the video of an MPEG system is shown in Table 1 thru/or 4. "extention data" or "user data" is recorded on "extention and user data(i)" in Table 1.

[0103]

[Table 1]



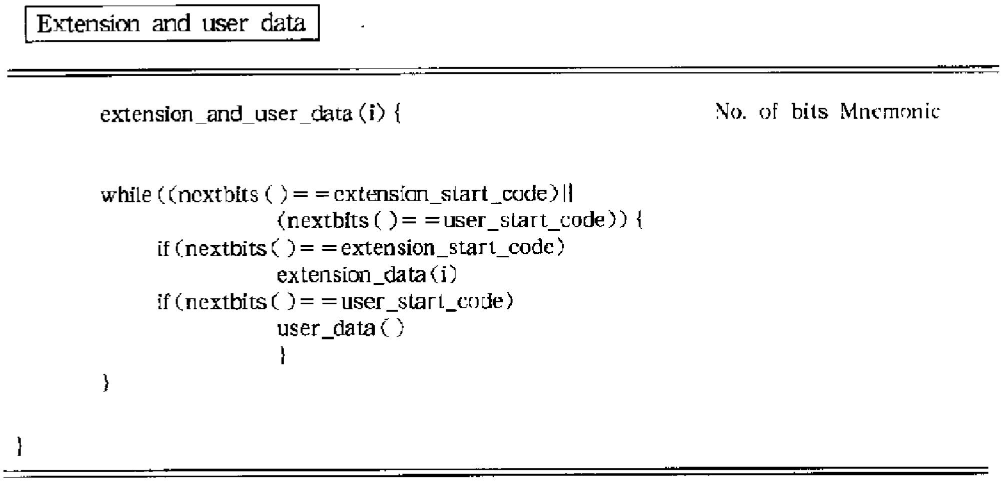
Video Sequence

```
video_sequence ( ) {
        next_start_code ( )
        sequence_header ( )
        if (nextbits ( ) = = extention_start_code) {      ........ MPEG 2  シンタックス
                  sequence_extension ( )
                  do {
                           extension_and_user_data (0)
                           do {
                                    if (next_bits ( ) = = group_start_code) {
                                             group_of_pictures_header ( )
                                             extension_and_user_data (1)
                                    }
                                   picture_header ( )
                                   extensions_and_user_data (2)
                                   picture_data ( )
                          } while ((next_bits ( ) = = picture_start_code)||
                                   next_bits ( ) = = group_start_code))
                          if (nextbits ( ) ! = sequence_end_code) {
                                   sequence_header ( )
                                   sequence_extension ( )
                          }
                  } while (nextbits ( ) ! = sequence_end_code)
        } else {                                                 ........ MPEG1 シンタックス
                  do {
                           do {
                                   group_of_pictures_header ( )
                                   if (next_bits ( ) = = user_data_start_code)
                                            user_data ( )
                                   do {
                                        picture_header ( )
                                        if (next_bits ( ) = = user_data_start_code)
                                                  user_data ( )
                                            picture_data ( )
                                   } while (next_bits ( ) = = picture_start_code)
                           } while (next_bits ( ) = = group_start_code)
                          if (nextbits ( ) ! = sequence_end_code)
                                   sequence_header ( )
                  } while (nextbits ( ) ! = sequence_end_code)
        }
      sequence_end_code
}
```

[0104]"extention and user data(i)" of Table 1 is shown in Table 2. When "userdata start cord" is indicated here, it is shown that "user data" is indicated below.

[0105]

[Table 2]



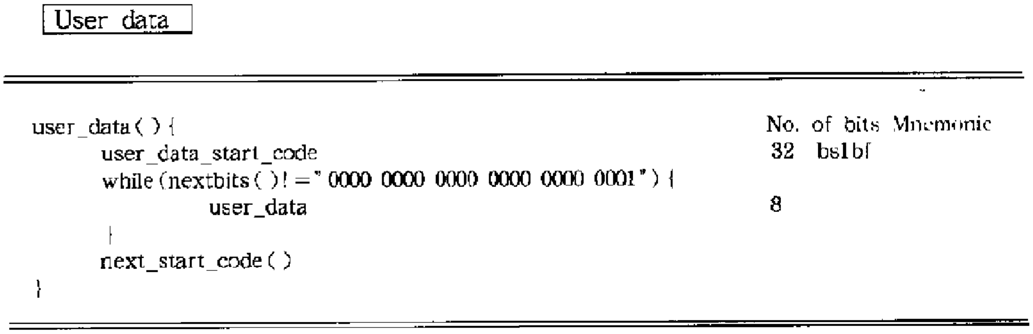
Extension and user data

```
extension_and_user_data (i) {                                    No. of bits Mnemonic


    while ((nextbits ( ) = = extension_start_code) ||
                (nextbits ( ) = = user_start_code)) {
        if (nextbits ( ) = = extension_start_code)
                extension_data (i)
        if (nextbits ( ) = = user_start_code)
                user_data ( )
                }
    }

}
```

[0106]"user data" is shown in Table 3. "user data" is recorded by 8 bitwises. For example, generating of "0000 0000 0000 0000 0000 0001" will mean that "user data" is completed.

[0107]

[Table 3]



User data

```
user_data ( ) {                                                  No. of bits Mnemonic
    user_data_start_code                                          32  bslbf
    while (nextbits ( ) ! = " 0000 0000 0000 0000 0000 0001") {
            user_data                                             8
    }
    next_start_code ( )
}
```

[0108]A PST flag is memorized by ""user data", for example as an 8-bit flag. A PST flag is shown in Table 4. Here, the filters 1 and 2, --, N show the various filters of the postfilter 22, for example.

[0109]

[Table 4]

| PST | フィルタ群 |
|---|---|
| 00000000 | フィルタ 1 |
| 00000001 | フィルタ 2 |
| 00000002 | フィルタ 3 |
| 00000003 | フィルタ 4 |
| ⋮ | ⋮ |
| 11111111 | フィルタ N |

[0110]The same filter is used until it is possible to use the value until it next resets, namely, it resets, since a PST flag can be set up after a sequence, GOP, and a picture header.
[0111]It is also possible to set up a PST flag with a sequence flag, and it may be made to perform the re set in this case by a sequence, GOP, and "user data" after a picture header.
[0112]The bit stream memorized by the storage 3 is decrypted by the decoder 31. The composition of this decoder 31 is constituted like the decoder circuit 90 shown by the conventional example of drawing 19, as shown in drawing 3.
If a bit stream is inputted into the variable length decoding circuit 82 of the decoder circuit 90 via the receive buffer 81, a variable length code will be solved in this variable length decoding circuit 82.
The PST flag currently recorded on "user data" at this time is decoded, and it is transmitted to the postfilter 22 shown in drawing 1. The composition of the other decoders 31 and operation are the same as a conventional example.
[0113]The postfilter 22 chooses the median filter as various filters of the postfilter 22, a low pass filter, etc. with the PST flag decrypted in this way, for example. A median filter and a low pass filter can be made into the filter group which consists of two or more kinds of filters with a parameter.
[0114]As shown in drawing 4, specifically the postfilter 22, Based on the inputted PST flag, the filter 100 (1) - 100 (N) are chosen with the switches 101 and 102, The signal which outputted to the filter which chose the color-difference signal C and the luminance signal Y which were memorized by the frame memories 34 and 35 as a bit stream, and was processed by the selected filter is outputted to D/A converters 36 and 37 via the switches 103 and 104.
[0115]Next, the median filter as an example of the filter of the postfilter 22 is explained. A median filter is a filter from which block distortion and a mosquito noise are removed effectively. As shown in drawing 5, the circumference of a certain pixel memorized by the field memory group 120, for example, 3x3 pixels, is taken out, put in order and changed in the 3x3-pixel extracting circuit 121, and it arranges and changes into ******** in the circuit 122.

Although the value of that center, i.e., the case of 3x3 pixels, calls the 5th value a median at this time, the Median detector 123 detects this median value, and it outputs to D/A converters 36 and 37 as a value of that pixel. The pixel value for asking for a median uses the pixel value before covering a filter.

[0116]In calculation of the above-mentioned median, although 3x3 pixels of circumferences of a certain pixel are used, the pixel group which asks not only for this but for a median may be set up how. And the effect of a filter is changeable by changing the pixel group which asks for this median.

[0117]For example, when the median filter which takes the median of 3x3 pixels about all the pixels is covered, block distortion can be removed, but it becomes a powerful filter used as the picture which faded to the whole (filter 1).

[0118]On the other hand, when the median filter which takes the median of 3x3 pixels is covered only over block edge, block distortion is removed, and compared with the filter 1, a high frequency component is maintainable (filter 2).

[0119]Although a one-dimensional median filter can be covered and the efficiency of block distortion removal falls compared with the filters 1 and 2 in this case, some high frequency components are maintainable (filter 3).

[0120]Such filters 1, 2, and 3 are switched with a PST flag, and an optimum filter is chosen.

[0121]Thus, according to image data coding and the decoding device of the 1st working example, based on the inputted PST flag, an optimum filter can be chosen by switching the switches 101 and 102 by the postfilter 22.

[0122]Next, the 2nd working example ****** explanation is given. Since the 2nd working example is almost the same as the 1st working example, a different point is a point which the setting method of a PST flag sets up based on the various parameters generated at the time of coding and other composition is the same as the 1st working example, only different composition is explained, the same numerals are attached to an identical configuration, and explanation is omitted.

[0123]In the PST flag deciding method in the encoder 18 of the 2nd working example. As shown in drawing 6, the filter which the postfilter selection circuitry 140 uses for post-processing according to the generation bit amount (encoding parameter) outputted from the various parameters and the bit counter which are inputted into the variable-length-coding machine circuit 58 is determined. The postfilter selection circuitry 140 outputs the PST flag which shows the postfilter to be used again to the variable-length-coding circuit 58. The variable-length-coding circuit 58 carries out variable length coding of the PST flag like the 1st working example.

[0124]Next, one example of the deciding method of the PST flag by the encoder 18 is explained. When you need especially the postfilter 22, it is a low bit rate, and it is when encoding efficiency is bad. In this case, block distortion, a mosquito noise, etc. appear notably and degradation of a picture becomes intense. Post-processing which stops being conspicuous in degradation of such a picture is needed. On the other hand, since the picture with sufficient encoding efficiency coded with the high bit rate is maintaining high definition while it had been decrypted, performing excessive post-processing will cause degradation of image quality on the contrary.

[0125]Therefore, the powerful filter from which block distortion etc. are removed needs to cover a filter with a more powerful sequence with worse encoding efficiency required, so that the coding bit rate is low.

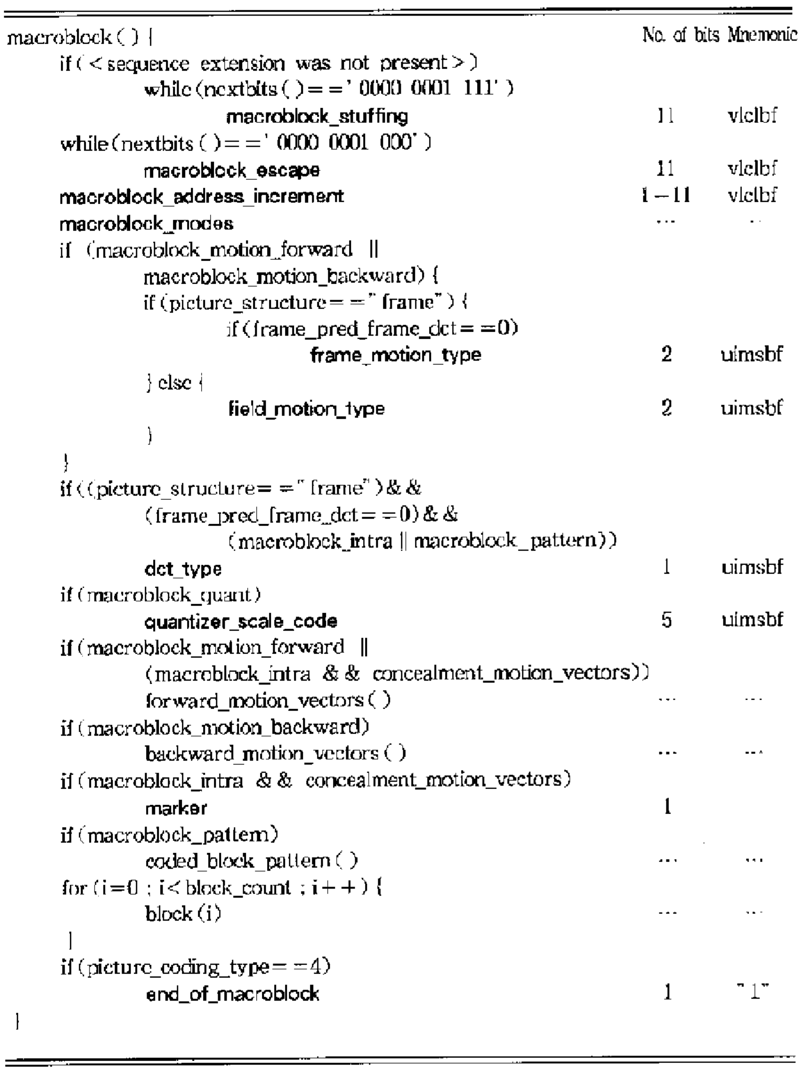
[0126]A quantization coefficient exists as an encoding parameter showing these. This quantization coefficient takes such a small value, and takes a value with a smaller sequence with more sufficient encoding efficiency that the coding bit rate becomes high. That is, what is necessary will be just to switch a PST flag accommodative according to the size of this quantization coefficient.

[0127]In the case of an MPEG system, a quantization coefficient (quantizer scale code) is set up by a macro block unit. Macro block syntax is shown in Table 5.

[0128]

[Table 5]

Macroblock layer



```
macroblock( ) |                                                  No. of bits Mnemonic
    if(<sequence extension was not present>)
            while(nextbits( )==' 0000 0001 111' )
                    macroblock_stuffing                              11       vlclbf
    while(nextbits( )==' 0000 0001 000' )
            macroblock_escape                                        11       vlclbf
    macroblock_address_increment                                     1-11     vlclbf
    macroblock_modes                                                 ...      ..
    if (macroblock_motion_forward ||
            macroblock_motion_backward) {
            if(picture_structure==" frame" ) {
                    if(frame_pred_frame_dct==0)
                            frame_motion_type                        2        uimsbf
            } else {
                    field_motion_type                                2        uimsbf
            }
    }
    if((picture_structure==" frame" )&&
            (frame_pred_frame_dct==0)&&
                    (macroblock_intra || macroblock_pattern))
            dct_type                                                 1        uimsbf
    if(macroblock_quant)
            quantizer_scale_code                                     5        uimsbf
    if(macroblock_motion_forward ||
            (macroblock_intra && concealment_motion_vectors))
            forward_motion_vectors( )                                ...      ...
    if(macroblock_motion_backward)
            backward_motion_vectors( )                               ...      ...
    if(macroblock_intra && concealment_motion_vectors)
            marker                                                   1
    if(macroblock_pattern)
            coded_block_pattern( )                                   ...      ...
    for(i=0 ; i< block_count ; i++) {
            block(i)                                                 ...      ...
     |
    if(picture_coding_type==4)
            end_of_macroblock                                        1        "1"
|
```

[0129]First, after one frame codes, average value MEAN_Q of the quantization coefficient in one frame is calculated. When such a filter powerful in a PST flag as shown in Table 4 that the value of a PST flag is large is supported, such a big PST flag is assigned that MEAN_Q is large. As the relation between MEAN_Q and a PST flag is shown in drawing 7 (A), even if it is linear relation, it may be a stair-like relation shown in drawing 7 (B) (drawing 7 (B) is the control system that a postfilter does not change frequently).

[0130]The relation between MEAN_Q and a PST flag shall be constituted using one of drawing 7 (A) and the (B), and shall have the same relation by the coding equipment and decoding device side.

[0131]As shown in drawing 8, specifically by the postfilter selection circuitry 140, an input of a quantizing scale (quantization coefficient) will compute MEAN_Q for every frame in the averaging circuit 150. And based on MEAN_Q, a PST flag is determined in the PST determining circuit 151, and it outputs to the variable-length-coding circuit 58. Other composition and an operation are the same as the 1st working example.

[0132]There is a method of using only the coding bit rate as modification of the method using the above-mentioned quantization coefficient, and a PST flag is set up after a sequence header in this case.

[0133]As explained above, since the 2nd working example is performing setting out of the PST flag based on the various parameters generated at the time of coding in addition to the effect of the 1st working example, it can set up the optimal PST flag according to the contents of coding, and can choose an optimum filter more.

[0134]Next, the 3rd working example ****** explanation is given. Since the 3rd working example is almost the same as the 2nd working example, a different point is a point of having formed the postfilter selection circuitry 140 which chooses a postfilter in the decoding device side and other composition is the same as the 2nd working example, only different composition is explained, the same numerals are attached to an identical configuration, and explanation is omitted.

[0135]As shown in drawing 9, the postfilter selection circuitry 140 provided in the encoder 18 of the coding equipment 1 is formed in the decoding device 2, and the 2nd working example constitutes it from the 3rd working example.

[0136]The decoder 31 of the 3rd working example is constituted like the decoder circuit 90 shown by the conventional example of drawing 19, as shown in drawing 10.

If a bit stream is inputted into the variable length decoding circuit 82 of the decoder circuit 90 via the receive buffer 81, a variable length code will be solved in this variable length decoding circuit 82.

The quantization coefficient as an encoding parameter is decrypted at this time, and it is transmitted to the postfilter 22. Other composition, an operation, and an effect are the same as the 2nd working example.

[0137]

[Effect of the Invention]Since the coding condition flag which shows the coding condition of a picture signal is coded according to the image processing method according to claim 1 when coding a picture signal based on an estimated image signal by an encoding means as more than explained, It is effective in the ability to amend a picture signal the optimal by easy composition, based on a coding condition flag when decoding a picture signal.

[0138]In the picture signal coding equipment according to claim 1, since a coding flag is set up based on the coding bit rate of the picture information of the bit stream which an encoding means codes by a flag setting means, it is effective in the ability to amend a picture signal to optimum more.

[0139]By amending the picture signal decrypted based on the coding condition flag which shows the coding condition of a picture signal by the picture compensation means according to the image signal decoding device according to claim 4. It is effective in the ability to amend a picture signal the optimal by easy composition, based on a coding condition flag when decoding a picture signal.

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[Translation done.]

CLAIMS DETAILED DESCRIPTION TECHNICAL FIELD PRIOR ART EFFECT OF THE INVENTION TECHNICAL PROBLEM MEANS EXAMPLE DESCRIPTION OF DRAWINGS DRAWINGS

[Translation done.]

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1.This document has been translated by computer. So the translation may not reflect the original precisely.
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3.In the drawings, any words are not translated.

## PRIOR ART

[Description of the Prior Art]When recording dynamic image data on a magneto-optical disc, magnetic tape, etc. in digital one, or when transmitting via a predetermined transmission medium, data is coded and compressed and data volume is made to decrease.
[0003]For example, like the video conference system and the video telephone system, in the system which transmits a dynamic image signal to a remote place, in order to use a transmission line efficiently, it is made as [ carry out / compression encoding of the picture signal ] using the line correlation and inter frame correlation of a video signal.
[0004]If line correlation is used, DCT (discrete cosine transform) processing can be carried out, for example, and a picture signal can be compressed.
[0005]If inter frame correlation is used, it will become possible to compress a picture signal further and to code. For example, as shown in drawing 11, when frame image PC1, PC2, and PC3 have occurred in the time t1, t2, and t3, respectively, The difference of the picture signal of the frame images PC1 and PC2 is calculated, PC12 is generated, and the difference of the frame images PC2 and PC3 is calculated, and PC23 is generated. Usually, since the picture of the frame which adjoins in time does not have a so big change, if both difference is calculated, the differential signal will become a thing of a small value. Then, a code amount is compressible if this differential signal is coded.
[0006]However, the original picture cannot be restored if only the differential signal was transmitted. Then, the picture of each frame is made into one picture of three kinds of pictures, I picture, P picture, or B picture, and it is made to carry out compression encoding of the picture signal.
[0007]That is, as shown, for example in drawing 12, frame F1 thru/or the picture signal of 17 frames to F17 are made into a glue PUOBU picture (GOP), and it may be one unit of processing. And the picture signal of frame F1 of the head is coded as an I picture, and the 2nd frame F2 processes the 3rd frame F3 as a B picture as a P picture, respectively.

Hereafter, the frames F4 thru/or F17 of the 4th henceforth are processed by turns as B picture or a P picture.

[0008]As a picture signal of I picture, the picture signal for the one frame is transmitted as it is. On the other hand, as a picture signal of P picture, fundamentally, as shown in drawing 12 (A), the difference from the picture signal of I picture or P picture preceded in time than it is transmitted. Furthermore, as a picture signal of B picture, fundamentally, as shown in drawing 12 (B), it asks for the difference from the average value of both the frame preceded in time or the frame which carries out backward, and the difference is coded.

[0009]Drawing 13 is carried out in this way, and the principle of the method of coding a dynamic image signal is shown. As shown in the figure, since the first frame F1 is processed as an I picture, it is transmitted to a transmission line as transmission data F1X as it is (formation of a picture inner code). On the other hand, since the 2nd frame F2 is processed as a B picture, the difference (prediction error) of frame F1 preceded in time and the average value of the frame F3 which carries out backward in time calculates, and the difference is transmitted as the transmission data F2X.

[0010]However, if the processing as this B picture is explained still more finely, they exist. [ four kinds of ] The 1st processing transmits the data of the original frame F2 as the transmission data F2X as it is, and turns into the same processing as the case in I picture (SP1) (intra (prediction within a picture) coding). The 2nd processing calculates the difference from the next frame F3 in time, and transmits the difference (SP2) (backward prediction coding). The 3rd processing transmits difference (SP3) with frame F1 preceded in time (forward prediction coding). Furthermore, the 4th processing generates difference (SP4) with the average value of the frame F3 which carries out backward to frame F1 preceded in time, and transmits this as the transmission data F2X (both-directions prediction coding).

[0011]The way transmission data decreases most among these four methods is adopted.

[0012]The motion vector x1 (frame F1 and motion vector between F2) (in the case of forward prediction) between the pictures (estimated image) of the frame which serves as an object which calculates difference when transmitting difference data, Or both x2 (motion vector between the frames F3 and F2) (in the case of backward prediction), or x1 and x2 (in the case of both-directions prediction) are transmitted with difference data.

[0013]A differential signal (SP3) with this frame and the motion vector x3 calculate the frame F3 of P picture by using as an estimated image frame F1 preceded in time, and this is transmitted as the transmission data F3X (forward prediction coding). Or the data of the original frame F3 is transmitted as the data F3X as it is again (intra coding). (SP1) As for whether it is transmitted by which method, the direction whose transmission data decreases more is chosen like the case in B picture.

[0014]Drawing 14 codes and transmits a dynamic image signal based on the principle mentioned above, and the example of composition of the device which decrypts this is shown. The coding equipment 1 codes the inputted video signal, and is made as [ transmit / to the recording medium 3 as a transmission line ]. And the decoding device 2 reproduces the signal recorded on the recording medium 3, and is made as [ output / this / decode and ].

[0015]In the coding equipment 1, the inputted video signal is inputted into the preprocessing circuit 11, a luminance signal and a chrominance signal (in the case of this working example color-difference signal) are separated there, and an A/D conversion is carried out with A/D converters 12 and 13, respectively. The video signal which the A/D conversion was carried out with A/D converters 12 and 13, and turned into a digital signal is supplied to the back frame memory 14 processed by the pre-filter 21, and is memorized. The frame memory 14 memorizes a luminance signal to the luminance-signal frame memory 15, and makes the color-difference-signal frame memory 16 memorize a color-difference signal, respectively.

[0016]The pre-filter 21 performs processing for raising encoding efficiency. This is for example, a noise rejection filter, and is a filter for restricting a zone.

[0017]The format conversion circuit 17 changes into the signal of a block format the signal of the frame format memorized by the frame memory 14. That is, as shown in drawing 15, let the video signal memorized by the frame memory 14 be the data of a frame format in which the lines of V lines of H dot were collected per line. The format conversion circuit 17 classifies this signal of one frame into N slices by making 16 lines into a unit. And each slice is divided into M macro blocks. Each macro block is constituted by the luminance signal corresponding to 16x16 pixels (dot), and this luminance signal is classified into block Y [1] which makes further 8x8 dots a unit thru/or Y [4]. And the Cb signal of 8x8 dots and the Cr signal of 8x8 dots are equivalent to this luminance signal of 16x16 dots.

[0018]Thus, the data changed into the block format is supplied to the encoder 18 from the format conversion circuit 17, and encoding (coding) is performed here. The details are later mentioned with reference to drawing 16.

[0019]The signal encoded by the encoder 18 is outputted to a transmission line as a bit stream. For example, the record circuit 19 is supplied and it is recorded on the recording medium 3 as a digital signal.

[0020]The data reproduced by the regenerative circuit 30 from the recording medium 3 is supplied to the decoder 31 of the decoding device 2, and is decoded. The details of the decoder 31 are later mentioned with reference to drawing 19.

[0021]The data decoded by the decoder 31 is inputted into the format conversion circuit 32, and is changed into a frame format from a block format. And the luminance signal of a frame format is supplied to the luminance-signal frame memory 34 of the frame memory 33, and is memorized, and a color-difference signal is supplied to the color-difference-signal frame memory 35, and is memorized. After being processed by the postfilter 22, D/A conversion of the luminance signal and color-difference signal which were read from the luminance-signal frame memory 34 and the color-difference-signal frame memory 35 is carried out by D/A converters 36 and 37, respectively, and they are supplied to the post-processing circuit 38, and are compounded. And for example, it is outputted and displayed on the display of CRT etc. which are not illustrated.

[0022]The postfilter 22 performs processing for improving image quality. For example, it is a filter for removing block distortion and a mosquito noise.

[0023]Next, the example of composition of the encoder 18 is explained with reference to drawing 16.

[0024]The image data which should be coded is inputted into the motion vector detection circuit 50 by a macro block unit. The motion vector detection circuit 50 processes the image data of each frame as I picture, P picture, or a B picture according to the predetermined sequence set up beforehand. Whether the picture of each frame inputted sequentially is processed as which picture of I, P, and B. it is set beforehand (for example, the glue PUOBU picture constituted by frame F1 thru/or F17 as shown in drawing 15 -- I, B, P, B, P, and ... processed as B and P).

[0025]The image data of the frame (for example, frame F1) processed as an I picture, The image data of the frame (for example, frame F2) which is transmitted and memorized by the front original image part 51a of the frame memory 51 from the motion vector detection circuit 50, and is processed as a B picture, The reference original image part 51b transmits and memorizes, and the image data of the frame (for example, frame F3) processed as a P picture is transmitted and memorized by the back original image part 51c.

[0026]When the picture of the frame which should be further processed as B picture (frame F4) or a P picture (frame F5) is inputted in the following timing, The image data of the first P picture (frame F3) memorized by the back original image part 51c till then, It is transmitted to the front original image part 51a, the image data of the following B picture (frame F4) is memorized by the reference original image part 51b (overwrite), and the image data of the following P picture (frame F5) is memorized by the back original image part 51c (overwrite). Such operation is repeated successively.

[0027]The signal of each picture memorized by the frame memory 51 is read from there, and frame prediction mode processing or field prediction mode processing is performed in the prediction mode switching circuit 52. In the operation part 53, the operation of the prediction within a picture, forward prediction, backward prediction, or both-directions prediction is performed under control of the prediction decision circuit 54 further again. It is determined corresponding to a prediction error signal (difference of the image comparison made into the object of processing, and the estimated image to this) whether to perform processing [ which ] among these processings. For this reason, the motion vector detection circuit 50 generates the absolute value sum (the sum of squares may be sufficient) of the prediction error signal used for this judgment.

[0028]Here, the frame prediction mode and field prediction mode in the prediction mode switching circuit 52 are explained.

[0029]When frame prediction mode is set up, the prediction mode switching circuit 52 outputs four luminosity block Y [1] supplied from the motion vector detection circuit 50 thru/or Y [4] to the latter operation part 53 as it is. Namely, it is in the state where the data of the line of an odd number field and the data of the line of an even number field were intermingled in each luminosity block, as [ show / in drawing 8 ] in this case. In this frame prediction mode, prediction is performed by making four luminosity blocks (macro block) into a unit, and one motion vector corresponds to four luminosity blocks.

[0030]On the other hand, the prediction mode switching circuit 52, As shown in drawing 17 (B), the signal inputted from the motion vector detection circuit 50 in field prediction mode with the composition shown in drawing 17 (A), Accept luminosity block Y [1] and Y [2], for example by the dot of the line of an odd number field, and they are made to constitute among four luminosity blocks, the data of the line of an even number field is made to constitute other two luminosity block Y [3] and Y [4], and they are outputted to the operation part 53. In this case, one motion vector corresponds to two luminosity block Y [1] and Y [2], and other one motion vector corresponds to other two luminosity block Y [3] and Y [4].

[0031]The motion vector detection circuit 50 outputs the absolute value sum of the prediction error in frame prediction mode, and the absolute value sum of the prediction error in field prediction mode to the prediction mode switching circuit 52. The prediction mode switching circuit 52 compares the absolute value sum of the prediction error in frame prediction mode and field prediction mode, performs processing corresponding to the prediction mode in which the value is small, and outputs data to the operation part 53.

[0032]However, such processing is performed actually in the motion vector detection circuit 50. That is, the motion vector detection circuit 50 outputs the signal of the composition corresponding to the determined mode to the prediction mode switching circuit 52, and the prediction mode switching circuit 52 outputs the signal to the latter operation part 53 as it is.

[0033]In the case of frame prediction mode, as shown in drawing 17 (A), a color-difference signal is in the state where the data of the line of an odd number field and the data of the line of an even number field are intermingled, and is supplied to the operation part 53. In the case of field prediction mode, as shown in drawing 17 (B), each color difference block Cb and the upper half (four lines) of Cr, It is considered as the color-difference signal of the odd number field corresponding to luminosity block Y [1] and Y [2], and a lower half (four lines) is made into the color-difference signal of the even number field corresponding to luminosity block Y [3] and Y [4].

[0034]The motion vector detection circuit 50 generates [ in / as follows / the prediction decision circuit 54 ] the absolute value sum of the prediction error for determining whether to perform prediction [ which / of the prediction within a picture, forward prediction, backward prediction, or both-directions prediction ].

[0035]That is, the difference of peace sigma|Aij | of absolute value |sigmaAij| of peace sigmaAij of the signal Aij of the macro block of an image comparison and absolute value |Aij| of the signal Aij of a macro block is searched for as an absolute value sum of the prediction error of the prediction within a picture. It asks for peace sigma|Aij-Bij [ of absolute value |Aij-Bij| of difference Aij-Bij of the signal Aij of the macro block of an image comparison, and the signal Bij of the macro block of an estimated image ] | as an absolute value sum of the prediction error of forward prediction. It asks for the absolute value sum of the prediction error of backward prediction and both-directions prediction as well as (changing the estimated image into a different estimated image from the case in forward prediction) the case in forward prediction.

[0036]These absolute value sums are supplied to the prediction decision circuit 54. The prediction decision circuit 54 chooses the smallest thing as an absolute value sum of the prediction error of the Inta prediction among the absolute value sums of the prediction error of forward prediction, backward prediction, and both-directions prediction. The absolute value sum of the prediction error of this Inta prediction is compared with the absolute value sum of the prediction error of the prediction within a picture, the smaller one of it is chosen, and the mode corresponding to this selected absolute value sum is chosen as prediction mode. That is, if the absolute value sum of the prediction error of the prediction within a picture is smaller, the prediction mode within a picture will be set up. If the absolute value sum of the prediction error of the Inta prediction is smaller, the mode whose absolute value sum corresponding among forward prediction, backward prediction, or both-directions prediction mode was the smallest will be set up.

[0037]Thus, the motion vector detection circuit 50 is the composition corresponding to the mode chosen by the prediction mode switching circuit 52 among a frame or field prediction mode in the signal of the macro block of an image comparison, While supplying the operation part 53 via the prediction mode switching circuit 52, the motion vector between the estimated image corresponding to the prediction mode in which the prediction decision circuit 54 was selected among four prediction modes, and an image comparison is detected, and it outputs to the variable-length-coding circuit 58 and the motion compensation circuit 65. As mentioned above, that from which the corresponding absolute value sum of a prediction error serves as the minimum as this motion vector is chosen.

[0038]When the motion vector detection circuit 50 has read the image data of I picture from the front original image part 51a in the prediction decision circuit 54, As prediction mode, a frame or field (picture) inner prediction mode (mode in which a motion compensation is not performed) is set up, and the switch 53d of the operation part 53 is changed to the point-of-contact a side. Thereby, the image data of I picture is inputted into the DCT mode switching circuit 55.

[0039]As shown in drawing 18 (A) or drawing 18 (B), this DCT mode switching circuit 55, The data of four luminosity blocks is changed into the state (frame DCT mode) where the line of an odd number field and the line of an even number field are intermingled or the separated state (field DCT mode), and the state of ********, and is outputted to DCT circuit 56.

[0040]That is, the DCT mode switching circuit 55 compares the encoding efficiency at the time of being intermingled and carrying out DCT processing of the data of an odd number field and an even number field with the encoding efficiency at the time of carrying out DCT processing in the state where it dissociated, and chooses the mode with good encoding efficiency.

[0041]For example, the inputted signal is considered as the composition in which the line of an odd number field and an even number field is intermingled as shown in drawing 18 (A), the difference of the signal of the line of an odd number field and the signal of the line of an even number field which adjoins up and down is calculated, and it asks for the sum (or sum of squares) of the absolute value further. The difference of the signal of the lines of the odd number field which considers the inputted signal as the composition which the line of an odd number field and an even number field separated as shown in drawing 18 (B), and adjoins up and down, The difference of the signal of the lines of an even number field is calculated, and it asks for the sum (or sum of squares) of each absolute value. Both (absolute value sum) are compared and the DCT mode corresponding to a small value is set up. That is, if former one is small, frame DCT mode will be set up, and if latter one is small, field DCT mode will be set up.

[0042]And while outputting the data of the composition corresponding to the selected DCT mode to DCT circuit 56, the DCT flag which shows the selected DCT mode is outputted to the variable-length-coding circuit 58, the DCT-blocks rearrangement circuit 62, and the motion compensation circuit 65.

[0043]The prediction mode (drawing 17) in the prediction mode switching circuit 52 is compared with the DCT mode (drawing 18) in this DCT mode switching circuit 55, and the data structure [ in / about a luminosity block / each mode of both ] is substantially the same so that clearly.

[0044]Also in [ when frame prediction mode (mode in which an odd line and an even line are intermingled) is chosen in the prediction mode switching circuit 52 ] the DCT mode switching circuit 55, In [ a possibility that frame DCT mode (mode in which an odd line and an even line are intermingled) will be chosen is high, and ] the prediction mode switching circuit 52, When field prediction mode (mode in which the data of an odd number field and an even number field was separated) is chosen, in the DCT mode switching circuit 55, a possibility that field DCT mode (mode in which the data of an odd number field and an even number field was separated) will be chosen is high.

[0045]However, it not necessarily always is not necessarily made such, the mode is determined that the absolute value sum of a prediction error will become small in the prediction mode switching circuit 52, and the mode is determined that encoding efficiency will become good in the DCT mode switching circuit 55.

[0046]It is inputted into DCT circuit 56, DCT (discrete cosine transform) processing is carried out, and the image data of I picture outputted from the DCT mode switching circuit 55 is changed into a DCT coefficient. This DCT coefficient is inputted into the variable-length-coding circuit 58, after being inputted into the quantization circuit 57 and quantized by the quantization step corresponding to the data accumulation amount (buffer accumulated dose) of the transmission buffer 59.

[0047]Corresponding to the quantization step (scale) supplied from the quantization circuit 57, the image data (in the case of now data of I picture) supplied from the quantization circuit 57 is changed into variable length codes, such as Huffman coding, for example, and the variable-length-coding circuit 58 outputs it to the transmission buffer 59.

[0048]In the variable-length-coding circuit 58, from the quantization circuit 57 again A quantization step (scale), the prediction decision circuit 54 -- prediction mode (the prediction within a picture, forward prediction, and backward prediction.) Any of both-directions prediction were set up from the mode and the motion vector detection circuit 50 which are shown Or a motion vector, From the prediction mode switching circuit 52, a prediction flag (flag which shows any should be set up between frame prediction mode or field prediction mode), And the DCT flag (flag which shows any should be set up between frame DCT mode or field DCT mode) which the DCT mode switching circuit 55 outputs is inputted, and variable length coding also of these is carried out.

[0049]The transmission buffer 59 stores the inputted data temporarily, and outputs the data corresponding to an accumulated dose to the quantization circuit 57. The transmission buffer 59 will reduce the data volume of quantization data by enlarging the quantizing scale of the quantization circuit 57 with a quantized control signal, if the data residue increases to permission upper limit. Contrary to this, if a data residue decreases to a permission lower limit, the transmission buffer 59 will increase the data volume of quantization data by making the quantizing scale of the quantization circuit 57 small with a quantized control signal. Thus, overflow or underflow of the transmission buffer 59 is prevented.

[0050]And the data stored in the transmission buffer 59 is read to predetermined timing, and is outputted to a transmission line, for example, is recorded on the recording medium 3.

[0051]On the other hand, the data of I picture outputted from the quantization circuit 57 is inputted into the inverse quantizing circuit 60, and inverse quantization is carried out corresponding to the quantization step supplied from the quantization circuit 57. The output of the inverse quantizing circuit 60 is inputted into the IDCT (reverse DCT) circuit 61, and after reverse DCT processing is carried out, it is inputted into the DCT-blocks rearrangement circuit 62. The DCT-blocks rearrangement circuit 62 performs a data list substitute corresponding to the prediction flag to which the inputted data is supplied from the prediction mode switching circuit 52, and the DCT flag supplied from the DCT mode switching circuit 55.

[0052]Namely, in the prediction mode switching circuit 52, when frame prediction mode is set up, it is in the state where the data of an odd number field and the data of an even number field are intermingled the data which is read from the motion compensation circuit 65 and supplied to the operation part 53. This data is supplied also to the computing unit 63. For this reason, the DCT-blocks rearrangement circuit 62, When frame DCT mode is set up in the data supplied from the IDCT circuit 61, Since it is in the state where the data of an odd number field and the data of the even number field were separated when the computing unit 63 is then supplied and field DCT mode is set up, data is rearranged into the state where these are intermingled and it outputs to the computing unit 63.

[0053]On the other hand, in the prediction mode switching circuit 52, when field prediction mode is set up, it is in the state where the data of an odd number field and the data of the even number field dissociated the data supplied to the operation part 53 from the motion compensation circuit 65. For this reason, the DCT-blocks rearrangement circuit 58 supplies the data outputted from the IDCT circuit 61 to the computing unit 63 as it is, when field DCT mode is set up by the DCT mode switching circuit 55, but. Since it is in the state where the data of an odd number field and the data of an even number field are intermingled when frame DCT mode is set up, each rearranges this into the state where it dissociated, and outputs it to the computing unit 63.

[0054]That is, the DCT-blocks rearrangement circuit 58 performs the data list substitute which the IDCT circuit 61 outputs so that it may be from the motion compensation circuit 65 in the same array state as the array state of the data supplied to the operation part 53.

[0055]Since the data which is outputted from the IDCT circuit 61 in now is data of I picture, it is considered as the prediction within a picture. For this reason, while the DCT mode switching circuit 55 is outputting the frame DCT flag, as it is, via the computing unit 63, the data outputted from the IDCT circuit 61 is supplied to the forward prediction picture part 65a of the frame memory 65, and is memorized. It memorizes, after a data list substitute is performed, when the field DCT flag is outputted.

[0056]The motion vector detection circuit 50 the image data of each frame inputted sequentially, For example, I, B, P, B, P, B ... When processing as a picture, respectively, After processing the image data of the frame inputted first as an I picture, before processing the picture of the frame inputted into the next as a B picture, the image data of the frame further inputted into the next is processed as a P picture. It is because it cannot decode unless P picture as a backward prediction image is prepared previously, in order to accompany B picture by backward prediction.

[0057]Then, the motion vector detection circuit 50 is processing of I picture, next starts processing of the image data of P picture memorized by the back original image part 51c. And the absolute value sum of the inter-frame difference (prediction error) in a macro block unit is supplied to the prediction mode switching circuit 52 and the prediction decision circuit 54 from the motion vector detection circuit 50 like the case where it mentions above. The prediction mode switching circuit 52 and the prediction decision circuit 54 set up the prediction mode of a frame / field prediction mode or the prediction within a picture, forward prediction, backward prediction, or both-directions prediction corresponding to the absolute value sum of the prediction error of the macro block of this P picture.

[0058]When the prediction mode within a picture is set up, the operation part 53 is changed to the point-of-contact a side, as the switch 53d was mentioned above. Therefore, this data is transmitted to a transmission line like the data of I picture via the DCT mode switching circuit 55, DCT circuit 56, the quantization circuit 57, the variable-length-coding circuit 58, and the transmission buffer 59. Via the inverse quantizing circuit 60, the IDCT circuit 61, the DCT-blocks rearrangement circuit 62, and the computing unit 63, this data is supplied to the backward prediction picture part 64b of the frame memory 64, and is memorized.

[0059]While the switch 53d is changed to the point of contact b at the time of forward prediction mode, The picture (in case of now picture of I picture) data memorized by the forward prediction picture part 64a of the frame memory 64 is read, and a motion compensation is carried out by the motion compensation circuit 65 corresponding to the motion vector which the motion vector detection circuit 50 outputs. Namely, when it is ordered the motion compensation circuit 65 in setting out in forward prediction mode from the prediction decision circuit 54, Only the part corresponding to the position lost-motion vector corresponding to the position of the macro block to which the motion vector detection circuit 50 is outputting the reading address of the forward prediction picture part 64a now is shifted, data is read, and prediction image data is generated.

[0060]The prediction image data outputted from the motion compensation circuit 65 is supplied to the computing unit 53a. The computing unit 53a subtracts the prediction image data corresponding to this macro block supplied from the motion compensation circuit 65 from the data of the macro block of the image comparison supplied from the prediction mode switching circuit 52, and outputs that difference (prediction error). This difference data is transmitted to a transmission line via the DCT mode switching circuit 55, DCT circuit 56, the quantization circuit 57, the variable-length-coding circuit 58, and the transmission buffer 59. This difference data is locally decoded by the inverse quantizing circuit 60, the IDCT circuit 61, and the DCT-blocks rearrangement circuit 62, and is inputted into the computing unit 63.

[0061]The same data as the prediction image data currently supplied to the computing unit 53a is supplied to this computing unit 63 again. The computing unit 63 adds the prediction image data which the motion compensation circuit 65 outputs to the difference data which the DCT-blocks rearrangement circuit 62 outputs. Thereby, the image data of the original P (it decoded) picture is obtained. The image data of this P picture is supplied to the backward prediction picture part 64b of the frame memory 64, and is memorized.

[0062]In this way, the motion vector detection circuit 50 performs processing of B picture next, after the data of I picture and P picture is memorized by the forward prediction picture part 64a and the backward prediction picture part 64b, respectively. The prediction mode switching circuit 52 and the prediction decision circuit 54, Corresponding to the size of the absolute value sum of the inter-frame difference in a macro block unit, a frame/field mode is set up and prediction mode is set to either the prediction mode within a picture, forward prediction mode, backward prediction mode or both-directions prediction mode.

[0063]As mentioned above, the switch 53d is changed to the point of contact a or b at the time of the prediction mode within a picture, or forward prediction mode. At this time, the same processing as the case in P picture is performed, and data is transmitted.

[0064]On the other hand, when backward prediction mode or both-directions prediction mode is set up, the switch 53d is changed to the point of contact c or d, respectively.

[0065]It is read by the picture (in case of now picture of P picture) data memorized by the backward prediction picture part 64b at the time of the backward prediction mode in which the switch 53d is changed to the point of contact c, and by the motion compensation circuit 65. A motion compensation is carried out corresponding to the motion vector which the motion vector detection circuit 50 outputs. Namely, when it is ordered the motion compensation circuit 65 in setting out in backward prediction mode from the prediction decision circuit 54, Only the part corresponding to the position lost-motion vector corresponding to the position of the macro block to which the motion vector detection circuit 50 is outputting the reading address of the backward prediction picture part 64b now is shifted, data is read, and prediction image data is generated.

[0066]The prediction image data outputted from the motion compensation circuit 65 is supplied to the computing unit 53b. The computing unit 53b subtracts the prediction image data supplied from the motion compensation circuit 65 from the data of the macro block of the image comparison supplied from the prediction mode switching circuit 52, and outputs the difference. This difference data is transmitted to a transmission line via the DCT mode switching circuit 55, DCT circuit 56, the quantization circuit 57, the variable-length-coding circuit 58, and the transmission buffer 59.

[0067]The picture (in case of now picture of I picture) data memorized by the forward prediction picture part 64a at the time of the both-directions prediction mode in which the switch 53d is changed to the point of contact d, The picture (in case of now picture of P picture) data memorized by the backward prediction picture part 64b is read, and a motion compensation is carried out by the motion compensation circuit 65 corresponding to the motion vector which the motion vector detection circuit 50 outputs. Namely, when it is ordered the motion compensation circuit 65 in setting out in both-directions prediction mode from the prediction decision circuit 54, The reading address of the forward prediction picture part 64a and the backward prediction picture part 64b, The motion vector detection circuit 50 shifts only the part corresponding to the position lost-motion vector (the motion vector in this case is set to two, the object for forward prediction pictures, and the object for backward prediction pictures) corresponding to the position of the macro block outputted now, reads data, and generates prediction image data.

[0068]The prediction image data outputted from the motion compensation circuit 65 is supplied to the computing unit 53c. The computing unit 53c subtracts the average value of the prediction image data supplied from the motion compensation circuit 65 from the data of the macro block of the image comparison supplied from the motion vector detection circuit 50, and outputs the difference. This difference data is transmitted to a transmission line via the DCT mode switching circuit 55, DCT circuit 56, the quantization circuit 57, the variable-length-coding circuit 58, and the transmission buffer 59.

[0069]Since the picture of B picture is not used as the estimated image of other pictures, it is not memorized by the frame memory 64.

[0070]In the frame memory 64, bank switching is performed if needed, and to a predetermined image comparison, the forward prediction picture part 64a and the backward prediction picture part 64b can change what is memorized on one side or another side as a forward prediction picture or a backward prediction picture, and can output it.

[0071]Although explained above focusing on the luminosity block, also about a color difference block, it is processed as a unit and the macro block shown in drawing 15 and the same macro block are transmitted. What set to one half the motion vector of the luminosity block with which the motion vector in the case of processing a color difference block corresponds to the perpendicular direction and the horizontal direction, respectively is used.

[0072]Drawing 19 is a block diagram showing the composition of the decoder circuit 90 which is one working example of the decoder 31 of drawing 14. After being received in the receiving circuit which is not illustrated, or being reproduced in a regenerative circuit and storing temporarily the coded image data which was transmitted via the transmission line (recording medium 3) at the receive buffer 81, it is supplied to the variable length decoding circuit 82 of the decoder circuit 90. The variable length decoding circuit 82 carries out variable-length decryption of the data supplied from the receive buffer 81, While outputting a motion vector, prediction mode, a prediction flag, and a DCT flag to the motion compensation circuit 88 and outputting a quantization step (scale) to the inverse quantizing circuit 83, respectively, the decoded image data is outputted to the inverse quantizing circuit 83. A DCT flag and a prediction flag are outputted to the inverse quantizing circuit 83.

[0073]The inverse quantizing circuit 83 carries out inverse quantization of the image data supplied from the variable length decoding circuit 82 according to the quantization step similarly supplied from the variable length decoding circuit 82, and outputs it to the IDCT circuit 84. The data (DCT coefficient) outputted from the inverse quantizing circuit 83 is the IDCT circuit 84, and reverse DCT processing is carried out and it is returned to the original image data.

[0074]This image data is further inputted into the DCT-blocks rearrangement circuit 86. Corresponding to a DCT flag and a prediction flag, the DCT-blocks rearrangement circuit 86 rearranges so that it may be in the same array state as the data which the motion compensation circuit 88 outputs to the operation part 87, and it outputs this data to the computing unit 87.

[0075]When the image data supplied from the DCT-blocks rearrangement circuit 86 is data of I picture, The data is outputted from the computing unit 86, for prediction-image-data generation of the image data (data of P picture or B picture) behind inputted into the computing unit 86, is supplied to the forward prediction picture part 87a of the frame memory 87, and is memorized. This data is outputted to the format conversion circuit 32 (drawing 14).

[0076]The image data supplied from the IDCT circuit 84 is data of P picture which uses the image data in front of one of them as prediction image data, When it is data in forward prediction mode, the image data (data of I picture) before [ one ] the forward prediction picture part 87a of the frame memory 87 memorizes is read, and the motion compensation corresponding to the motion vector outputted from the variable length decoding circuit 82 in the motion compensation circuit 88 is given. And in the computing unit 86, it is added with the image data (data of difference) supplied from the DCT-blocks rearrangement circuit 86, and is outputted. For prediction-image-data generation of the image data (data of B picture or P picture) behind inputted into the computing unit 86, this added data, i.e., the decoded data of P picture, is supplied to the backward prediction image part 87b of the frame memory 87, and it is memorized.

[0077]Even if it is data of P picture, as for the data in the prediction mode within a picture, like the data of I picture, the computing unit 87 does not perform processing in particular, but the backward prediction picture part 87b memorizes as it is.

[0078]Since this P picture is a picture which should be displayed on the next of the following B picture, it is not outputted to the format conversion circuit 32 yet at this time (as mentioned above, P picture inputted after B picture is processed ahead of B picture, and is transmitted).

[0079]When the image data supplied from the DCT-blocks rearrangement circuit 86 is data of

B picture, it corresponds to the prediction mode supplied from the variable length decoding circuit 82, The image data of I picture memorized by the forward prediction picture part 87a of the frame memory 87 (in the case of forward prediction mode), The image data of P picture memorized by the backward prediction picture part 87b (in the case of backward prediction mode), Or the image data (in the case of both-directions prediction mode) of the both is read, the motion compensation corresponding to the motion vector outputted from the variable length decoding circuit 82 is given in the motion compensation circuit 88, and an estimated image is generated. However, an estimated image is not generated when you do not need a motion compensation (in the case of the prediction mode within a picture).

[0080]Thus, the data in which the motion compensation was given is added with DCT-blocks rearrangement circuit 86 output in the computing unit 86 in the motion compensation circuit 88. This added output is outputted to the format conversion circuit 32.

[0081]However, this added output is data of B picture, and since it is not used for estimated image generation of other pictures, it is not memorized by the frame memory 87.

[0082]After the picture of B picture is outputted, the image data of P picture memorized by the backward prediction picture part 87b is read, and the format conversion circuit 32 is supplied via the motion compensation circuit 88 and the computing unit 86. However, a motion compensation is not performed at this time.

[0083]Although the circuit corresponding to the prediction mode switching circuit 52 and the DCT mode switching circuit 55 in the encoder 18 of drawing 16 is not illustrated by this decoder 31, The motion compensation circuit 88 performs processing which returns the processing corresponding to these circuits, i.e., the composition from which the signal of the line of an odd number field and an even number field was separated, to the intermingled original composition if needed.

[0084]Although processing of the luminance signal was explained above, it is similarly carried out about the treatment of a color-difference signal. However, that to which the motion vector set the thing for luminance signals to one half to the perpendicular direction and the horizontal direction is used.

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[Translation done.]

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## EFFECT OF THE INVENTION

[Effect of the Invention]Since the coding condition flag which shows the coding condition of a picture signal is coded according to the image processing method according to claim 1 when coding a picture signal based on an estimated image signal by an encoding means as more than explained, It is effective in the ability to amend a picture signal the optimal by easy composition, based on a coding condition flag when decoding a picture signal.
[0138]In the picture signal coding equipment according to claim 1, since a coding flag is set up based on the coding bit rate of the picture information of the bit stream which an encoding means codes by a flag setting means, it is effective in the ability to amend a picture signal to optimum more.
[0139]By amending the picture signal decrypted based on the coding condition flag which shows the coding condition of a picture signal by the picture compensation means according to the image signal decoding device according to claim 4. It is effective in the ability to amend a picture signal the optimal by easy composition, based on a coding condition flag when decoding a picture signal.

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## TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]When it has the postfilter 22 like the decoding device shown in drawing 14, various kinds of filters exist in the postfilter 22, but it is dependent on the character of image quality, and the conditions at the time of coding what kind of filter is the optimal.
[0086]For example, since degradation of the decrypted picture is remarkable when the coding bit rate is low, in order to compensate this, it is necessary to cover the filter for improving image quality strongly. On the other hand, when the coding bit rate is high, the decrypted picture remains as it is, high definition is maintained and the same filter as the case of a low bit rate is used, there is a problem of making image quality deteriorate by that cause.
[0087]A pacey picture has bad encoding efficiency, for example, considering only the case of a low bit rate, since degradation becomes remarkable at image quality, it is necessary to cover the filter for improving image quality strongly but, and when this is used for a picture with sufficient encoding efficiency, there is a problem of worsening image quality on the contrary.
[0088]That is, there is a problem that the conventional image data can be compressed and image data cannot be elongated the optimal corresponding to the character of image quality or the conditions at the time of coding with numerals and the image signal processor to decrypt.
[0089]In light of the above-mentioned circumstances, this invention is a thing.
The purpose is to provide the picture signal coding equipment and the image signal decoding device which can amend the picture signal which was boiled and was decrypted more the optimal.

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## MEANS

[Means for Solving the Problem]In picture signal coding equipment with which the picture signal coding equipment according to claim 1 was provided with the encoder 18 as an encoding means which codes a picture signal based on a predetermined estimated image signal, When coding a picture signal based on an estimated image signal, the encoder 18 is constituted so that a coding condition flag which shows a coding condition of a picture signal may be coded.
[0091]The picture signal coding equipment according to claim 1 makes a picture signal picture information of a bit stream, A coding flag is made to exist in user area of said picture information of a bit stream, and it can have the postfilter selection circuitry 140 as a flag setting means which sets up a coding flag based on the coding bit rate of picture information of a bit stream which the encoder 18 codes.
[0092]In an image signal decoding device to decrypt, an image signal decoding device of Claim 4 a coded image signal which coded a picture signal based on a predetermined estimated image signal a coded image signal, It consists of a coding condition flag which shows a coding condition of a picture signal and a picture signal, and based on a coding condition flag, the postfilter 22 as a picture compensation means which amends a decrypted picture signal is provided, and it is constituted.
[0093]
[work --] for By coding a coding condition flag which shows a coding condition of a picture signal in the picture signal coding equipment according to claim 1, when coding a picture signal based on an estimated image signal with the encoder 18. It makes it possible to amend a picture signal the optimal by easy composition, based on a coding condition flag, when decoding a picture signal.
[0094]In the picture signal coding equipment according to claim 1, it makes it possible to amend a picture signal to optimum more by setting up a coding flag based on the coding bit

rate of picture information of a bit stream which the encoder 18 codes by the postfilter selection circuitry 140.

[0095]By amending a picture signal decrypted in an image signal decoding device of Claim 4 based on a coding condition flag which shows a coding condition of a picture signal by the postfilter 22. It makes it possible to amend a picture signal the optimal by easy composition, based on a coding condition flag, when decoding a picture signal.

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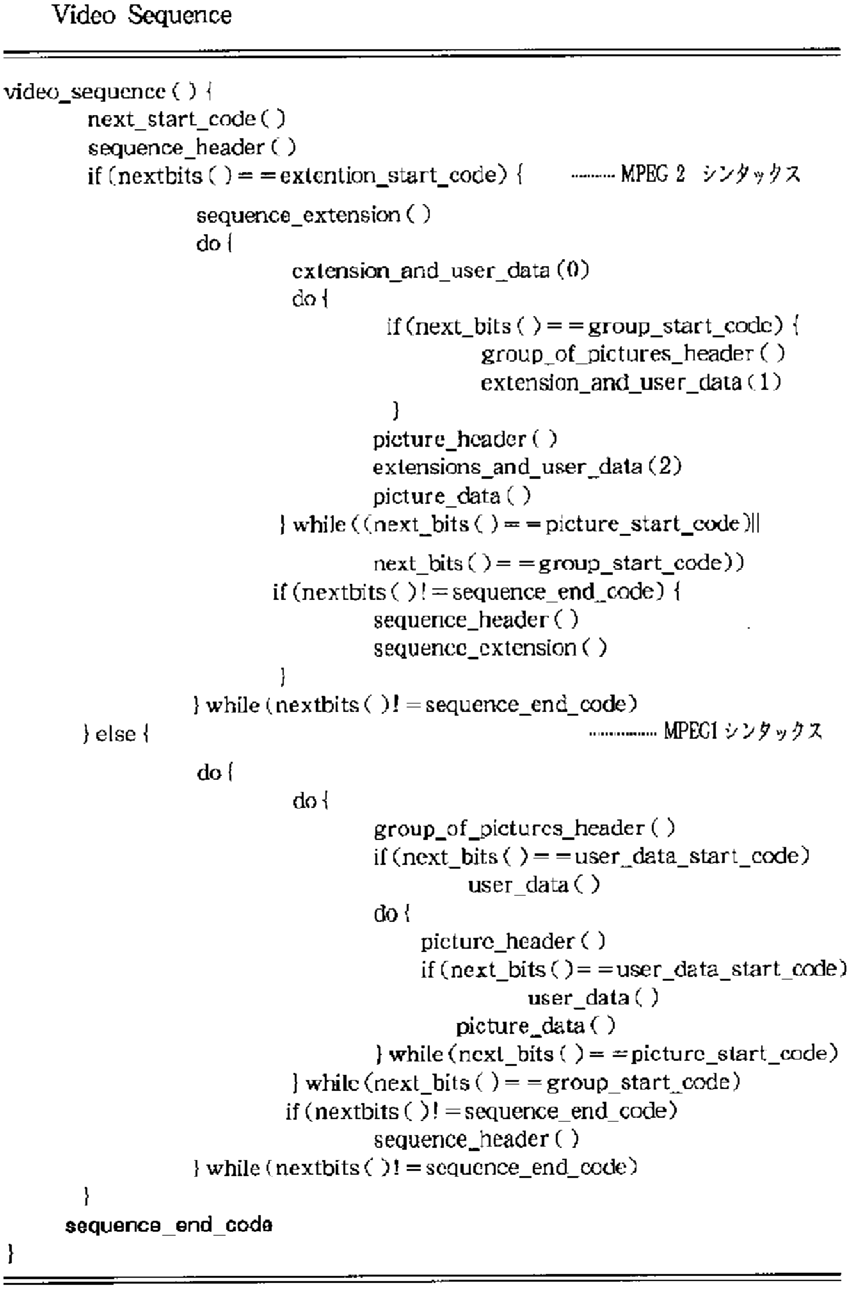
## EXAMPLE

[Example]Since the 1st working example of drawing 1 has the same composition as a conventional example, only different composition is explained, the same numerals are attached to an identical configuration, and explanation is omitted.
[0097]The image data coding equipment 1 and the image data decoding device 2 of the 1st working example, As the composition of the encoder 18, the decoder 31, and the postfilter 22 differs from a conventional example and it is shown in drawing 1, in this example the encoder 18 of the coding equipment 1, Simultaneously with the bit stream which is image data, the PST flag which shows the coding condition of the pre-filter 21 is coded, and a PST flag is transmitted to the recording medium 3 with a bit stream.
[0098]The bit stream and PST flag which were coded by the recording medium 3 and memorized are decrypted by the decoder 31 of the decoding device 2, and the decrypted bit stream is inputted into the format conversion circuit 32, and is changed into a frame format from a block format. On the other hand, the decrypted PST flag is transmitted to the postfilter 22, and chooses an optimum filter with a PST flag in the postfilter 22.
[0099]The determination of the PST flag by the encoder 18 is made by a method as shown below by this example. That is, it is the method of inputting and setting up a PST flag compulsorily from the outside, and the deciding method of this PST flag is explained.
[0100]The composition of the encoder 18 which realizes this deciding method is shown in drawing 2. The inputted PST flag is inputted into the variable-length-coding circuit 58. And in the variable-length-coding circuit 58, variable length coding of the bit stream is carried out like a conventional example, and variable length coding of the inputted PST flag is carried out.
[0101]And a PST flag is memorized by the storage 3 with a bit stream as the user datum (user data) in a bit stream. In MPEG and an MPEG2 system, since "user data" can be set up after a sequence, GOP, and a picture header, a PST flag can be similarly set up per a sequence, GOP, and picture header.

[0102]Here, the syntax of the video of an MPEG system is shown in Table 1 thru/or 4. "extention data" or "user data" is recorded on "extention and user data(i)" in Table 1.

[0103]

[Table 1]



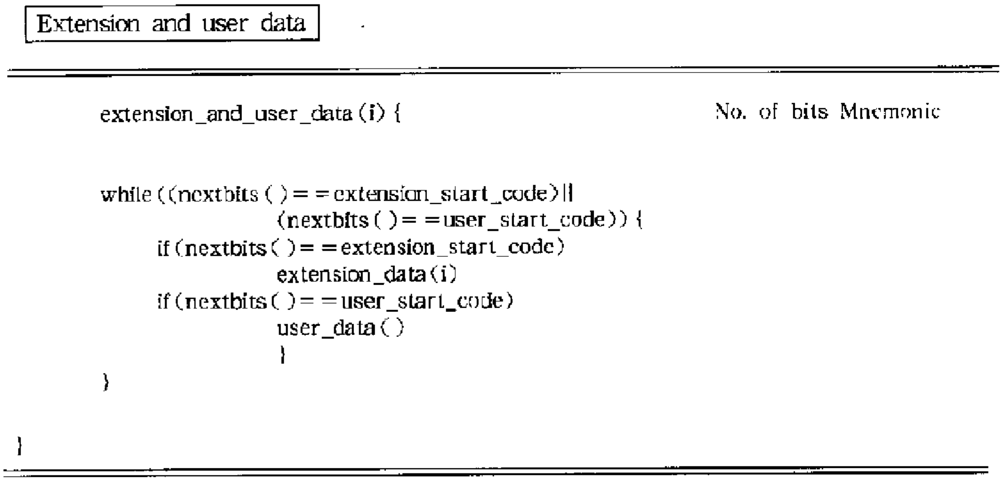
Video Sequence

```
video_sequence ( ) {
        next_start_code ( )
        sequence_header ( )
        if (nextbits ( ) = = extention_start_code) {        ·········MPEG 2  シンタックス
                  sequence_extension ( )
                  do {
                           extension_and_user_data (0)
                           do {
                                    if (next_bits ( ) = = group_start_code) {
                                             group_of_pictures_header ( )
                                             extension_and_user_data (1)
                                    }
                                  picture_header ( )
                                  extensions_and_user_data (2)
                                  picture_data ( )
                          } while ((next_bits ( ) = = picture_start_code)||
                                  next_bits ( ) = = group_start_code))
                          if (nextbits ( )! = sequence_end_code) {
                                  sequence_header ( )
                                  sequence_extension ( )
                          }
                  } while (nextbits ( )! = sequence_end_code)
        } else {                                                 ··············· MPEG1 シンタックス
                  do {
                           do {
                                  group_of_pictures_header ( )
                                  if (next_bits ( ) = = user_data_start_code)
                                           user_data ( )
                                  do {
                                       picture_header ( )
                                       if (next_bits ( ) = = user_data_start_code)
                                                 user_data ( )
                                          picture_data ( )
                                  } while (next_bits ( ) = = picture_start_code)
                           } while (next_bits ( ) = = group_start_code)
                          if (nextbits ( )! = sequence_end_code)
                                  sequence_header ( )
                  } while (nextbits ( )! = sequence_end_code)
        }
      sequence_end_code
}
```

[0104]"extention and user data(i)" of Table 1 is shown in Table 2. When "userdata start cord" is indicated here, it is shown that "user data" is indicated below.

[0105]

[Table 2]



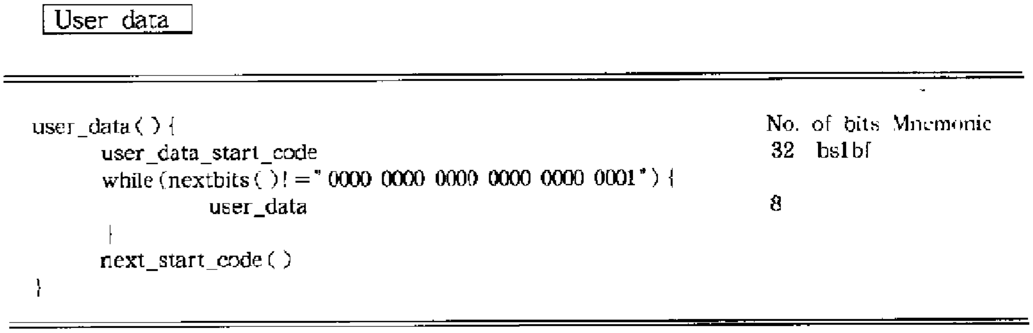
Extension and user data

```
extension_and_user_data(i) {                                   No. of bits Mnemonic

    while((nextbits()==extension_start_code)||
                    (nextbits()==user_start_code)) {
        if(nextbits()==extension_start_code)
                    extension_data(i)
        if(nextbits()==user_start_code)
                    user_data()
                    }
    }

}
```

[0106]"user data" is shown in Table 3. "user data" is recorded by 8 bitwises. For example, generating of "0000 0000 0000 0000 0000 0001" will mean that "user data" is completed.

[0107]

[Table 3]



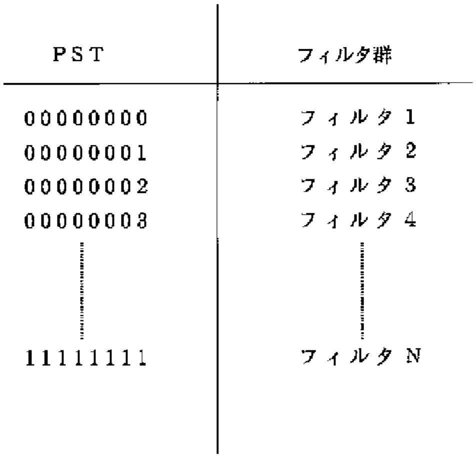
User data

```
user_data() {                                                  No. of bits Mnemonic
    user_data_start_code                                       32   bslbf
    while(nextbits()!=" 0000 0000 0000 0000 0000 0001") {
            user_data                                          8
    }
    next_start_code()
}
```

[0108]A PST flag is memorized by ""user data", for example as an 8-bit flag. A PST flag is shown in Table 4. Here, the filters 1 and 2, --, N show the various filters of the postfilter 22, for example.

[0109]

[Table 4]



| PST | フィルタ群 |
|---|---|
| 00000000 | フィルタ 1 |
| 00000001 | フィルタ 2 |
| 00000002 | フィルタ 3 |
| 00000003 | フィルタ 4 |
| ⋮ | ⋮ |
| 11111111 | フィルタ N |

[0110]The same filter is used until it is possible to use the value until it next resets, namely, it resets, since a PST flag can be set up after a sequence, GOP, and a picture header.

[0111]It is also possible to set up a PST flag with a sequence flag, and it may be made to perform the re set in this case by a sequence, GOP, and "user data" after a picture header.

[0112]The bit stream memorized by the storage 3 is decrypted by the decoder 31. The composition of this decoder 31 is constituted like the decoder circuit 90 shown by the conventional example of drawing 19, as shown in drawing 3.

If a bit stream is inputted into the variable length decoding circuit 82 of the decoder circuit 90 via the receive buffer 81, a variable length code will be solved in this variable length decoding circuit 82.

The PST flag currently recorded on "user data" at this time is decoded, and it is transmitted to the postfilter 22 shown in drawing 1. The composition of the other decoders 31 and operation are the same as a conventional example.

[0113]The postfilter 22 chooses the median filter as various filters of the postfilter 22, a low pass filter, etc. with the PST flag decrypted in this way, for example. A median filter and a low pass filter can be made into the filter group which consists of two or more kinds of filters with a parameter.

[0114]As shown in drawing 4, specifically the postfilter 22, Based on the inputted PST flag, the filter 100 (1) - 100 (N) are chosen with the switches 101 and 102, The signal which outputted to the filter which chose the color-difference signal C and the luminance signal Y which were memorized by the frame memories 34 and 35 as a bit stream, and was processed by the selected filter is outputted to D/A converters 36 and 37 via the switches 103 and 104.

[0115]Next, the median filter as an example of the filter of the postfilter 22 is explained. A median filter is a filter from which block distortion and a mosquito noise are removed effectively. As shown in drawing 5, the circumference of a certain pixel memorized by the field memory group 120, for example, 3x3 pixels, is taken out, put in order and changed in the 3x3-pixel extracting circuit 121, and it arranges and changes into ******** in the circuit 122.

Although the value of that center, i.e., the case of 3x3 pixels, calls the 5th value a median at this time, the Median detector 123 detects this median value, and it outputs to D/A converters 36 and 37 as a value of that pixel. The pixel value for asking for a median uses the pixel value before covering a filter.

[0116]In calculation of the above-mentioned median, although 3x3 pixels of circumferences of a certain pixel are used, the pixel group which asks not only for this but for a median may be set up how. And the effect of a filter is changeable by changing the pixel group which asks for this median.

[0117]For example, when the median filter which takes the median of 3x3 pixels about all the pixels is covered, block distortion can be removed, but it becomes a powerful filter used as the picture which faded to the whole (filter 1).

[0118]On the other hand, when the median filter which takes the median of 3x3 pixels is covered only over block edge, block distortion is removed, and compared with the filter 1, a high frequency component is maintainable (filter 2).

[0119]Although a one-dimensional median filter can be covered and the efficiency of block distortion removal falls compared with the filters 1 and 2 in this case, some high frequency components are maintainable (filter 3).

[0120]Such filters 1, 2, and 3 are switched with a PST flag, and an optimum filter is chosen.

[0121]Thus, according to image data coding and the decoding device of the 1st working example, based on the inputted PST flag, an optimum filter can be chosen by switching the switches 101 and 102 by the postfilter 22.

[0122]Next, the 2nd working example ****** explanation is given. Since the 2nd working example is almost the same as the 1st working example, a different point is a point which the setting method of a PST flag sets up based on the various parameters generated at the time of coding and other composition is the same as the 1st working example, only different composition is explained, the same numerals are attached to an identical configuration, and explanation is omitted.

[0123]In the PST flag deciding method in the encoder 18 of the 2nd working example. As shown in drawing 6, the filter which the postfilter selection circuitry 140 uses for post-processing according to the generation bit amount (encoding parameter) outputted from the various parameters and the bit counter which are inputted into the variable-length-coding machine circuit 58 is determined. The postfilter selection circuitry 140 outputs the PST flag which shows the postfilter to be used again to the variable-length-coding circuit 58. The variable-length-coding circuit 58 carries out variable length coding of the PST flag like the 1st working example.

[0124]Next, one example of the deciding method of the PST flag by the encoder 18 is explained. When you need especially the postfilter 22, it is a low bit rate, and it is when encoding efficiency is bad. In this case, block distortion, a mosquito noise, etc. appear notably and degradation of a picture becomes intense. Post-processing which stops being conspicuous in degradation of such a picture is needed. On the other hand, since the picture with sufficient encoding efficiency coded with the high bit rate is maintaining high definition while it had been decrypted, performing excessive post-processing will cause degradation of image quality on the contrary.

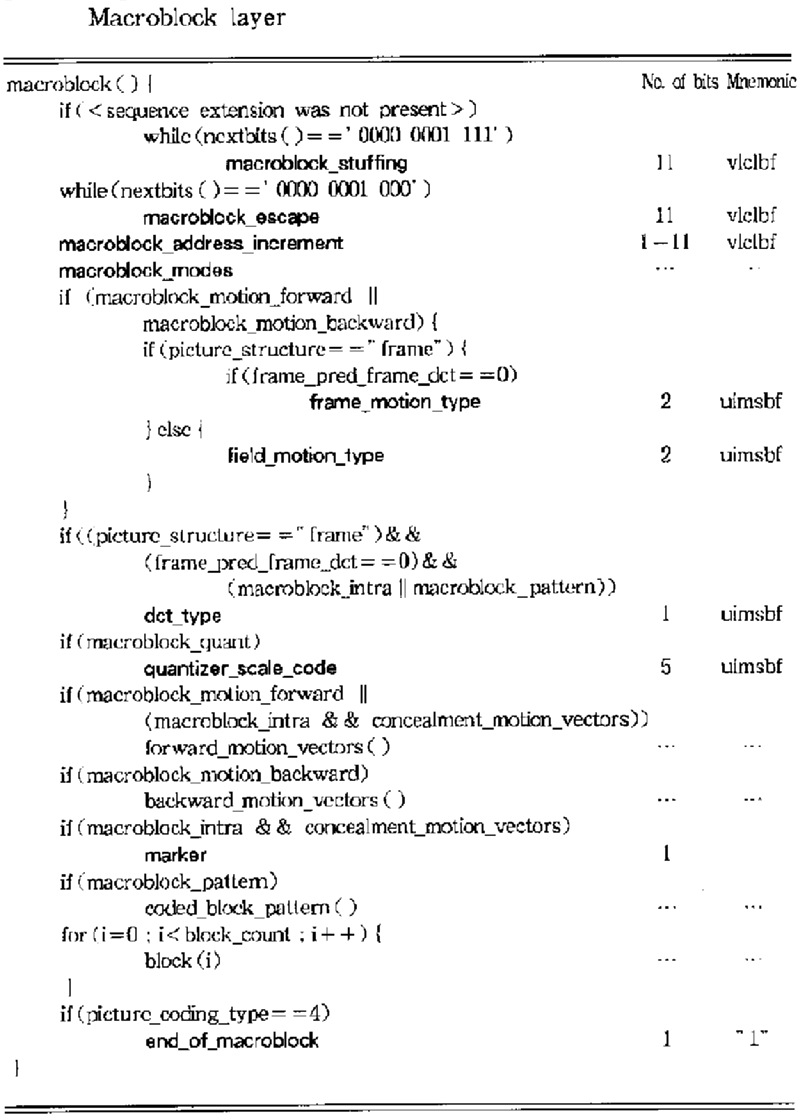
[0125]Therefore, the powerful filter from which block distortion etc. are removed needs to cover a filter with a more powerful sequence with worse encoding efficiency required, so that the coding bit rate is low.

[0126]A quantization coefficient exists as an encoding parameter showing these. This quantization coefficient takes such a small value, and takes a value with a smaller sequence with more sufficient encoding efficiency that the coding bit rate becomes high. That is, what is necessary will be just to switch a PST flag accommodative according to the size of this quantization coefficient.

[0127]In the case of an MPEG system, a quantization coefficient (quantizer scale code) is set up by a macro block unit. Macro block syntax is shown in Table 5.

[0128]

[Table 5]



Macroblock layer

```
macroblock() {                                                  No. of bits  Mnemonic
    if(<sequence extension was not present>)
        while(nextbits()==' 0000 0001 111')
            macroblock_stuffing                                     11       vlclbf
    while(nextbits()==' 0000 0001 000')
        macroblock_escape                                           11       vlclbf
    macroblock_address_increment                                  1-11       vlclbf
    macroblock_modes                                               ...       ..
    if (macroblock_motion_forward ||
        macroblock_motion_backward) {
        if(picture_structure==" frame") {
            if(frame_pred_frame_dct==0)
                frame_motion_type                                    2       uimsbf
        } else {
            field_motion_type                                        2       uimsbf
        }
    }
    if((picture_structure==" frame")&&
        (frame_pred_frame_dct==0)&&
            (macroblock_intra || macroblock_pattern))
        dct_type                                                     1       uimsbf
    if(macroblock_quant)
        quantizer_scale_code                                         5       uimsbf
    if(macroblock_motion_forward ||
        (macroblock_intra && concealment_motion_vectors))
        forward_motion_vectors()                                   ...       ...
    if(macroblock_motion_backward)
        backward_motion_vectors()                                  ...       ...
    if(macroblock_intra && concealment_motion_vectors)
        marker                                                       1
    if(macroblock_pattern)
        coded_block_pattern()                                      ...       ...
    for(i=0 ; i<block_count ; i++) {
        block(i)                                                   ...       ...
    }
    if(picture_coding_type==4)
        end_of_macroblock                                            1       "1"
}
```

[0129]First, after one frame codes, average value MEAN_Q of the quantization coefficient in one frame is calculated. When such a filter powerful in a PST flag as shown in Table 4 that the value of a PST flag is large is supported, such a big PST flag is assigned that MEAN_Q is large. As the relation between MEAN_Q and a PST flag is shown in drawing 7 (A), even if it is

linear relation, it may be a stair-like relation shown in drawing 7 (B) (drawing 7 (B) is the control system that a postfilter does not change frequently).
[0130]The relation between MEAN_Q and a PST flag shall be constituted using one of drawing 7 (A) and the (B), and shall have the same relation by the coding equipment and decoding device side.
[0131]As shown in drawing 8, specifically by the postfilter selection circuitry 140, an input of a quantizing scale (quantization coefficient) will compute MEAN_Q for every frame in the averaging circuit 150. And based on MEAN_Q, a PST flag is determined in the PST determining circuit 151, and it outputs to the variable-length-coding circuit 58. Other composition and an operation are the same as the 1st working example.
[0132]There is a method of using only the coding bit rate as modification of the method using the above-mentioned quantization coefficient, and a PST flag is set up after a sequence header in this case.
[0133]As explained above, since the 2nd working example is performing setting out of the PST flag based on the various parameters generated at the time of coding in addition to the effect of the 1st working example, it can set up the optimal PST flag according to the contents of coding, and can choose an optimum filter more.
[0134]Next, the 3rd working example ****** explanation is given. Since the 3rd working example is almost the same as the 2nd working example, a different point is a point of having formed the postfilter selection circuitry 140 which chooses a postfilter in the decoding device side and other composition is the same as the 2nd working example, only different composition is explained, the same numerals are attached to an identical configuration, and explanation is omitted.
[0135]As shown in drawing 9, the postfilter selection circuitry 140 provided in the encoder 18 of the coding equipment 1 is formed in the decoding device 2, and the 2nd working example constitutes it from the 3rd working example.
[0136]The decoder 31 of the 3rd working example is constituted like the decoder circuit 90 shown by the conventional example of drawing 19, as shown in drawing 10.
If a bit stream is inputted into the variable length decoding circuit 82 of the decoder circuit 90 via the receive buffer 81, a variable length code will be solved in this variable length decoding circuit 82.
The quantization coefficient as an encoding parameter is decrypted at this time, and it is transmitted to the postfilter 22. Other composition, an operation, and an effect are the same as the 2nd working example.

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## DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a block diagram showing the composition of the 1st working example of image data coding and decoding device of this invention.
[Drawing 2]It is a block diagram showing the composition of the encoder 18 of drawing 1.
[Drawing 3]It is a block diagram showing the composition of the decoder circuit 90 as the decoder 31 of drawing 1.
[Drawing 4]It is a block diagram showing the composition of the postfilter 22 of drawing 1.
[Drawing 5]It is a block diagram showing the composition of the median filter as an example of a filter of the postfilter 22 of drawing 4.
[Drawing 6]It is a block diagram showing the composition of the encoder 18 of the 2nd working example of this invention.
[Drawing 7]It is an explanatory view explaining an operation of the postfilter selection circuitry 140 of drawing 6.
[Drawing 8]It is a block diagram showing the composition of the postfilter selection circuitry 140 of drawing 6.
[Drawing 9]It is a block diagram showing the composition of the 3rd working example of image data coding and decoding device of this invention.
[Drawing 10]It is a block diagram showing the composition of the decoder circuit 90 as the decoder 31 of drawing 9.
[Drawing 11]It is a figure explaining the principle of high efficiency coding.
[Drawing 12]It is a figure explaining the type of the picture in the case of compressing image data.
[Drawing 13]It is a figure explaining the principle which codes a dynamic image signal.
[Drawing 14]It is a block diagram showing the example of composition of picture signal coding equipment and a decoding device.

[Drawing 15]It is a figure explaining operation of the format conversion of the format conversion circuit 17 in drawing 14.

[Drawing 16]It is a block diagram showing the example of composition of the encoder 18 in drawing 14.

[Drawing 17]It is a figure explaining operation of the prediction mode switching circuit 52 of drawing 16.

[Drawing 18]It is a figure explaining operation of the DCT mode switching circuit 55 of drawing 16.

[Drawing 19]It is a block diagram showing the example of composition of the decoder circuit 90 which is one example of the decoder 31 of drawing 14.

[Description of Notations]

1 Coding equipment
2 Decoding device
3 Recording medium
12, 13 A/D converters
14 Frame memory
15 Luminance-signal frame memory
16 Color-difference-signal frame memory
17 Format conversion circuit
18 Encoder
21 Pre-filter
22 Postfilter
31 Decoder
32 Format conversion circuit
33 Frame memory
34 Luminance-signal frame memory
35 Color-difference-signal frame memory
36, 37 D/A converters
49 Picture decision circuit
50 Motion vector detection circuit
51 Frame memory
52 Prediction mode switching circuit
53 Operation part
54 Prediction decision circuit
55 DCT mode switching circuit
56 DCT circuit
57 Quantization circuit

58 Variable-length-coding circuit
59 Transmission buffer
60 Inverse quantizing circuit
61 IDCT circuit
63 Computing unit
64 Frame memory
65 Motion compensation circuit
81 Receive buffer
82 Variable length decoding circuit
83 Inverse quantizing circuit
84 IDCT circuit
86 Computing unit
87 Frame memory
88 Motion compensation circuit
The 100(1) -100 (N) filter 1 - the filter N
101 and 102 Switch
121 3x3-pixel extracting circuit
122 Arrange and change and it is a circuit.
123 Median detector circuit
140 Postfilter detector circuit
150 Averaging circuit
151 PST determining circuit

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[Translation done.]

* NOTICES *

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damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

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## DRAWINGS

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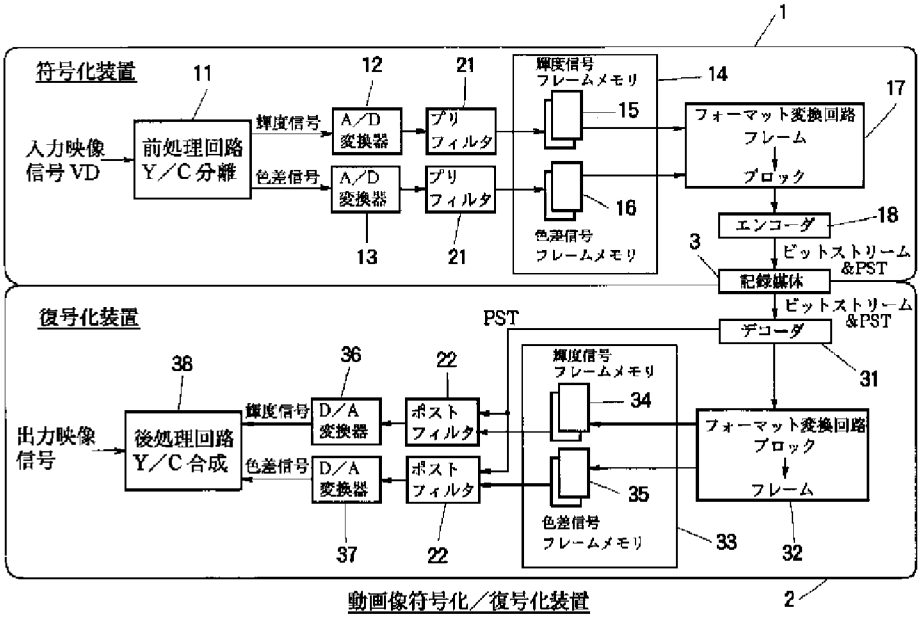
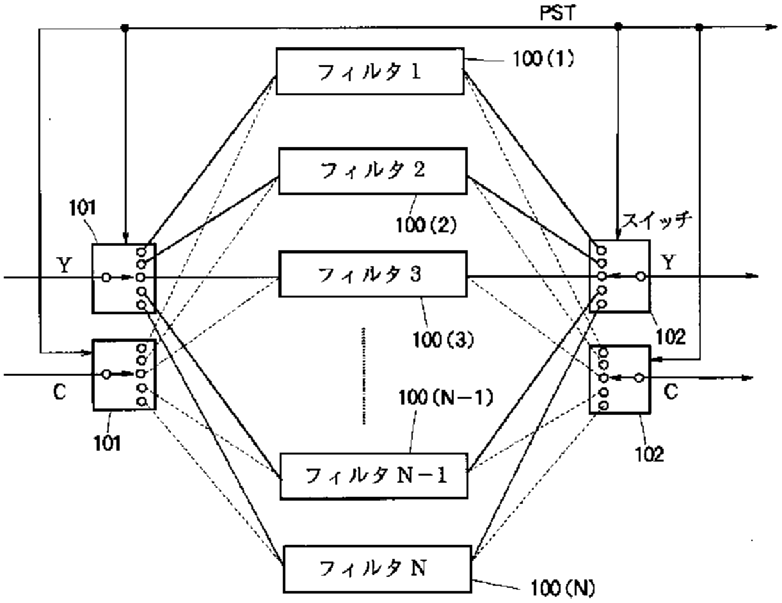
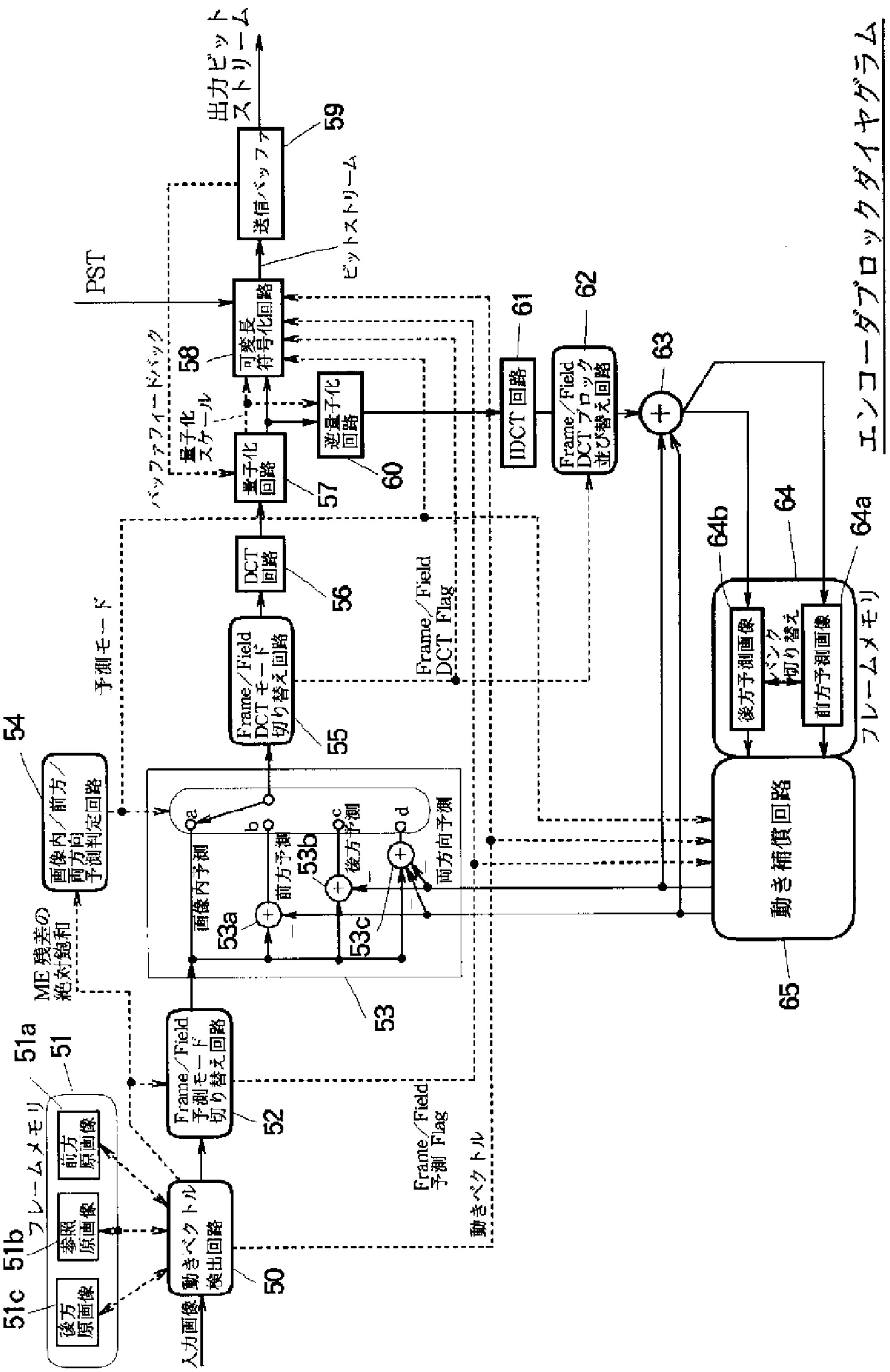
[Drawing 1]



[Drawing 4]

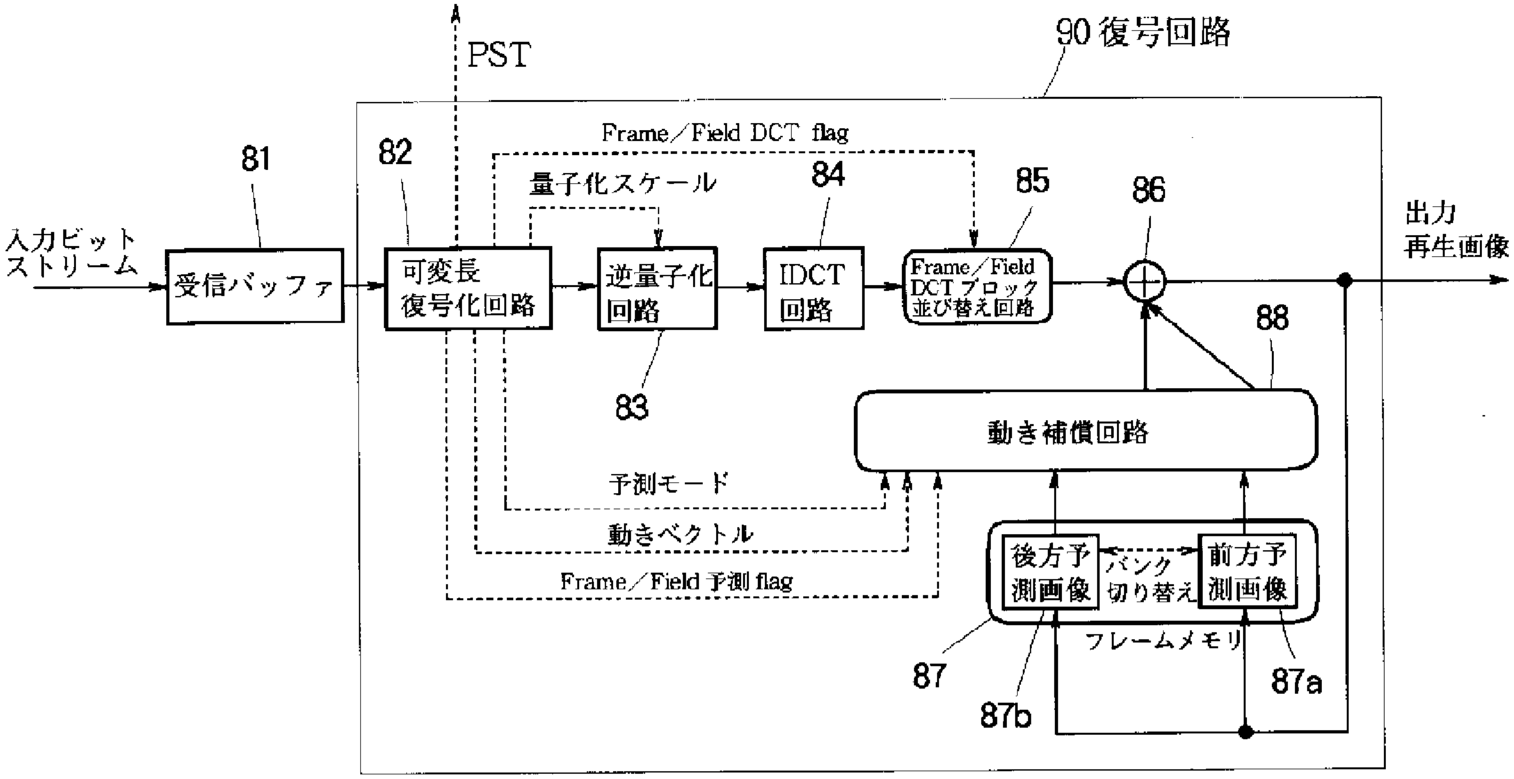

PST
フィルタ 1
100(1)
フィルタ 2
100(2)
101
スイッチ
Y
フィルタ 3
Y
100(3)
102
C
100(N−1)
C
101
102
フィルタ N−1
フィルタ N
100(N)

[Drawing 2]

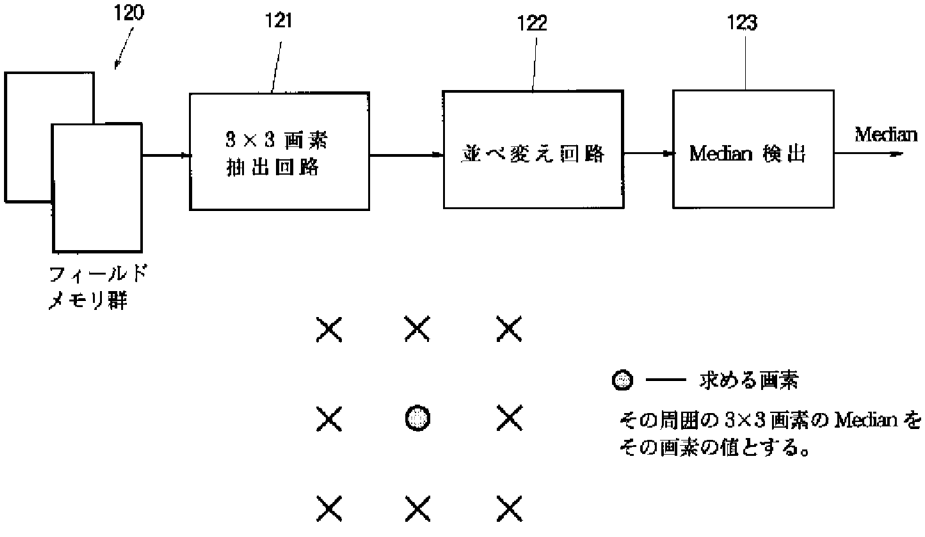

エンコーダブロックダイヤグラム
入力画像
動きベクトル検出回路
50
フレームメモリ
51
51a
前方原画像
51b
参照原画像
51c
後方原画像
Frame／Field予測モード切り替え回路
52
ME 残差の絶対値和
画像内／前方／両方向予測判定回路
54
予測モード
53
a
b
c
d
画像内予測
前方予測
後方予測
両方向予測
53a
53b
53c
Frame／Field DCTモード切り替え回路
55
DCT回路
56
量子化回路
57
量子化スケール
バッファフィードバック
可変長符号化回路
58
PST
送信バッファ
59
ビットストリーム
出力ビットストリーム
逆量子化回路
60
IDCT回路
61
Frame／Field DCTブロック並び替え回路
62
63
フレームメモリ
64
64a
前方予測画像
64b
後方予測画像
バンク切り替え
動き補償回路
65
Frame／Field 予測 Flag
Frame／Field DCT Flag
動きベクトル

[Drawing 3]

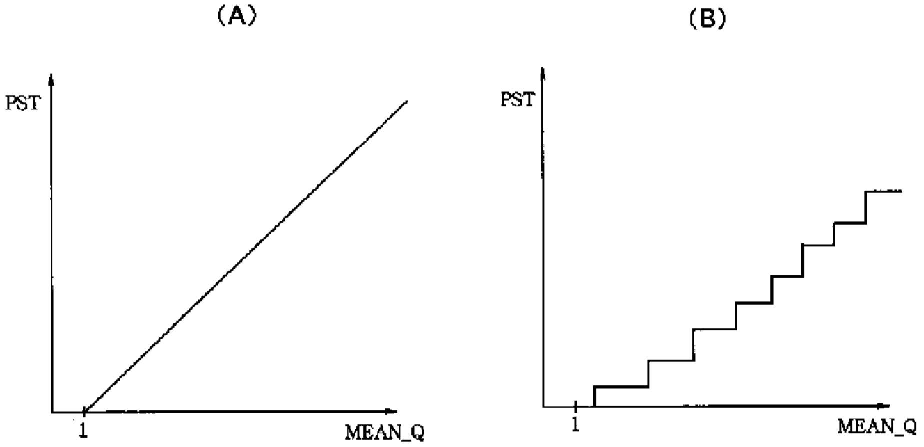
[Drawing 5]



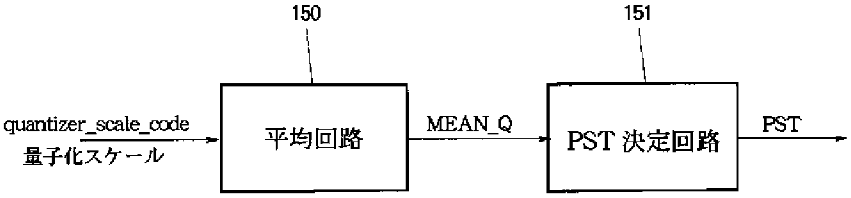
デコーダブロックダイヤグラム



## [Drawing 7]

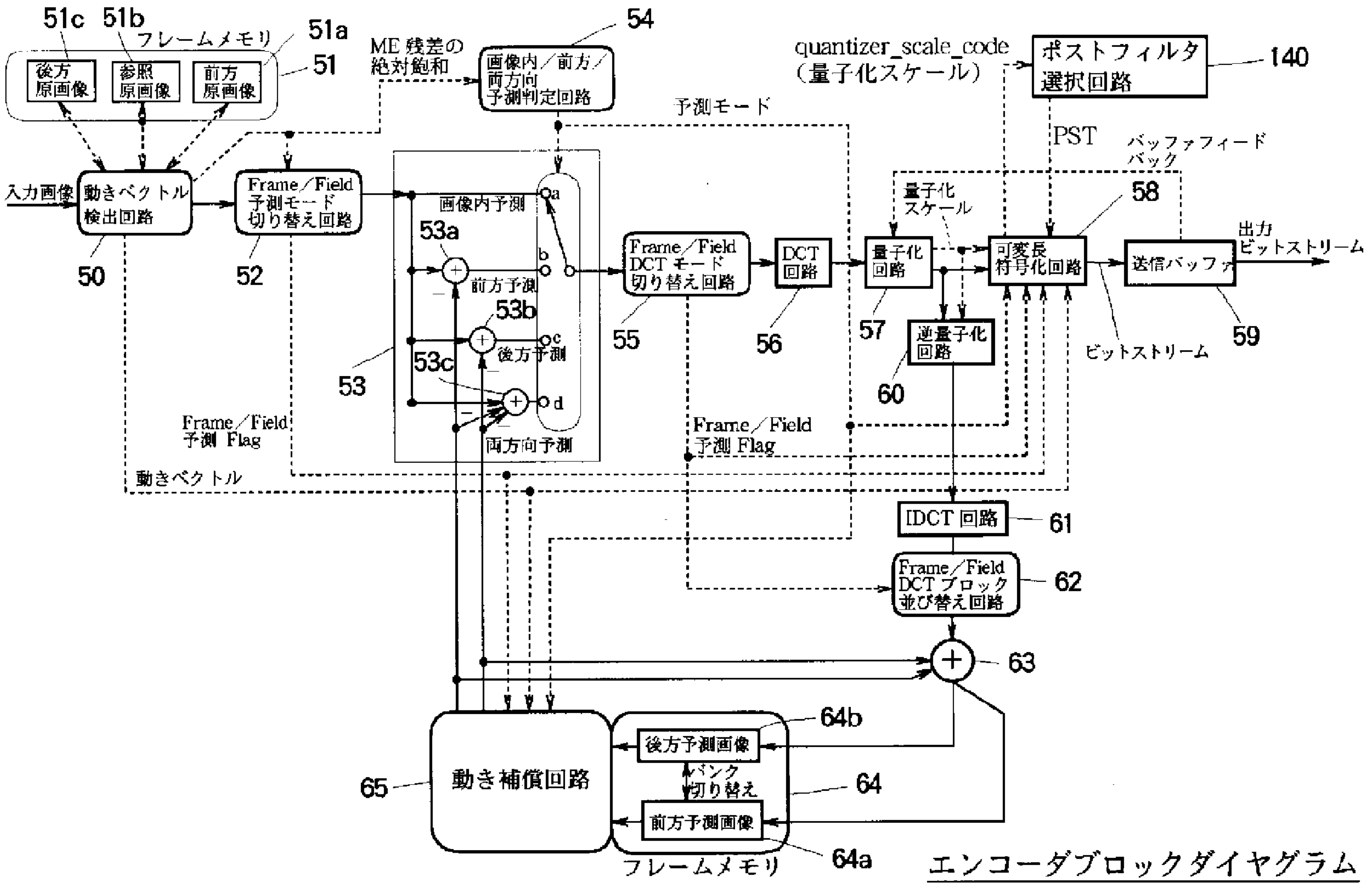


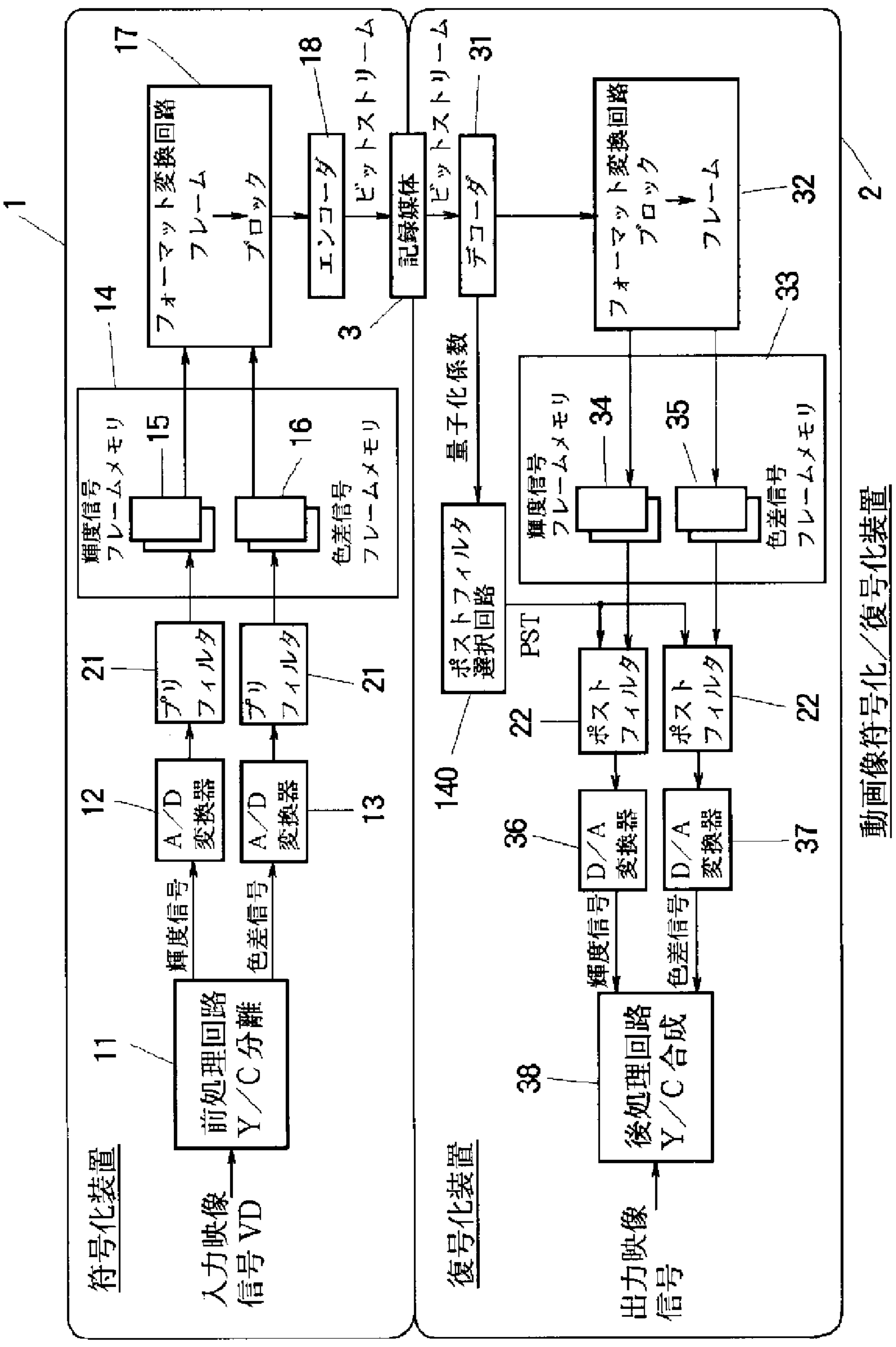
## [Drawing 8]



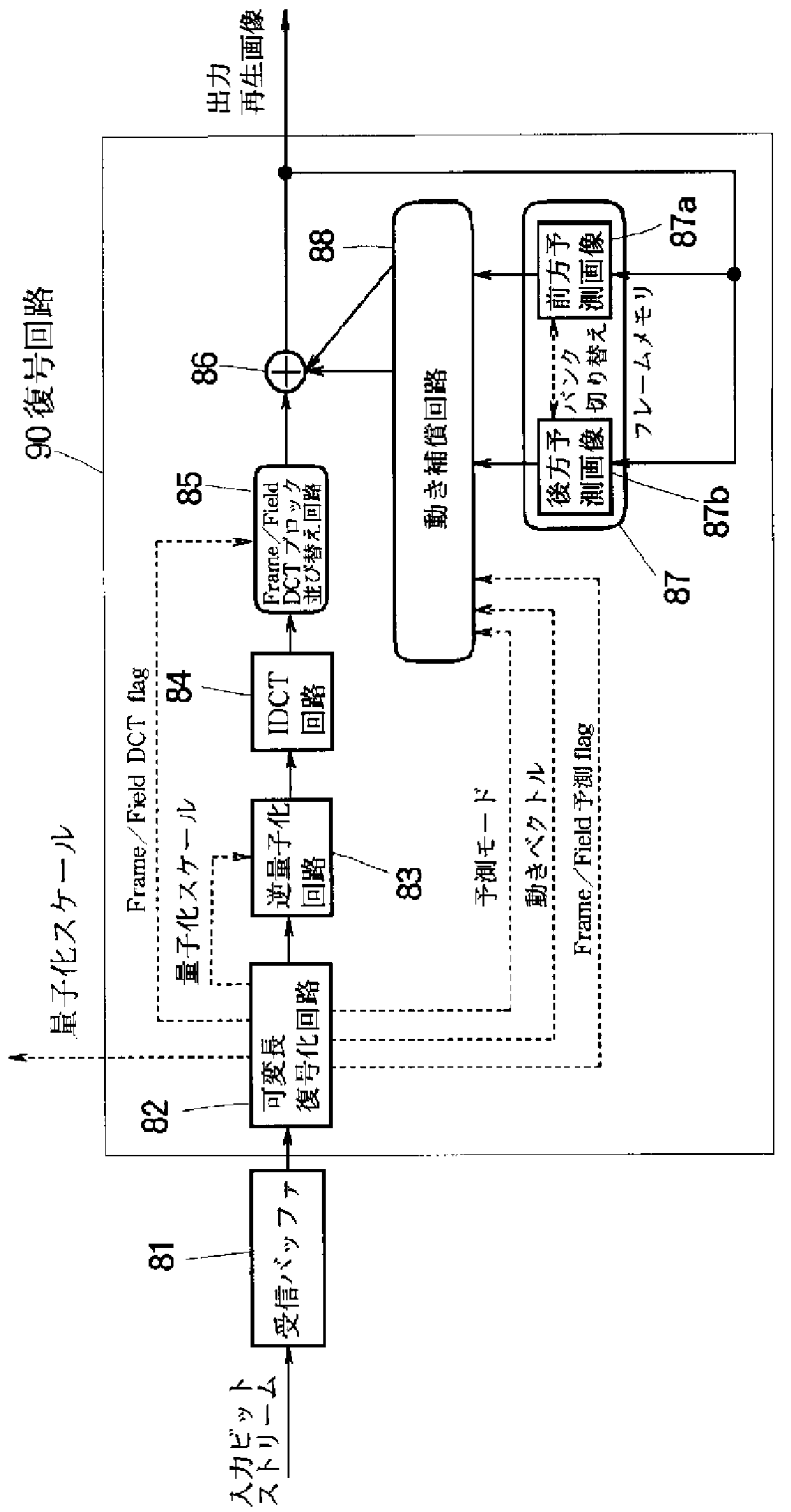
## [Drawing 6]

[Drawing 9]


51c
51b
フレームメモリ
51a
51
後方原画像
参照原画像
前方原画像
入力画像
動きベクトル検出回路
50
Frame／Field予測モード切り替え回路
52
ME 残差の絶対飽和
画像内／前方／両方向予測判定回路
54
予測モード
画像内予測
53a
前方予測
53b
後方予測
53c
両方向予測
a
b
c
d
53
Frame／Field DCT モード切り替え回路
55
DCT回路
56
量子化回路
57
量子化スケール
逆量子化回路
60
可変長符号化回路
58
quantizer_scale_code
（量子化スケール）
ポストフィルタ選択回路
140
PST
バッファフィードバック
送信バッファ
59
出力ビットストリーム
ビットストリーム
Frame／Field予測 Flag
動きベクトル
Frame／Field予測 Flag
IDCT 回路
61
Frame／Field DCT ブロック並び替え回路
62
63
64b
後方予測画像
バンク切り替え
64
前方予測画像
64a
フレームメモリ
動き補償回路
65
エンコーダブロックダイヤグラム

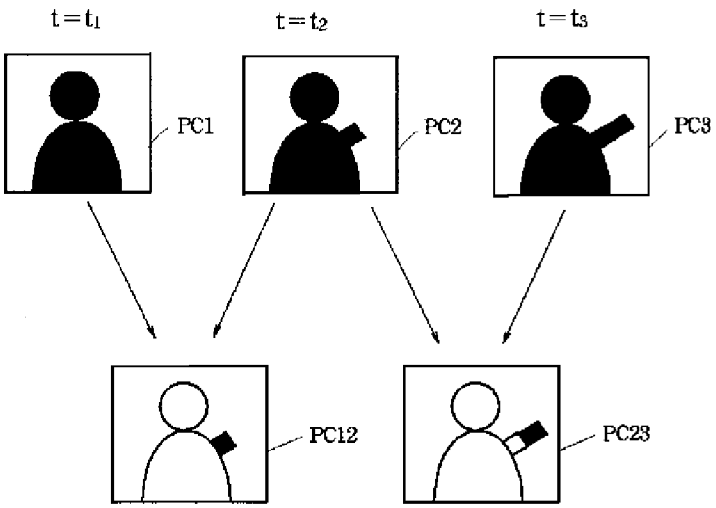

1
符号化装置
入力映像信号VD
11
前処理回路
Y/C分離
輝度信号
色差信号
12
A/D変換器
13
A/D変換器
21
プリフィルタ
21
プリフィルタ
14
15
輝度信号フレームメモリ
16
色差信号フレームメモリ
17
フォーマット変換回路
フレーム
ブロック
18
エンコーダ
ビットストリーム
3
記録媒体
ビットストリーム
31
デコーダ
32
フォーマット変換回路
ブロック
フレーム
2
33
34
輝度信号フレームメモリ
35
色差信号フレームメモリ
量子化係数
140
ポストフィルタ選択回路
PST
22
ポストフィルタ
22
ポストフィルタ
36
D/A変換器
37
D/A変換器
輝度信号
色差信号
38
後処理回路
Y/C合成
出力映像信号
復号化装置
動画像符号化/復号化装置

[Drawing 10]



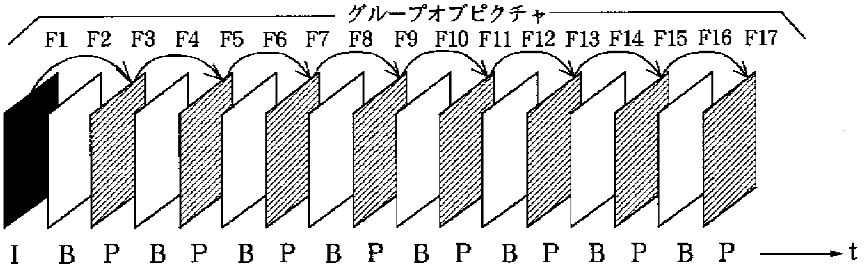
デコーダブロックダイヤグラム

[Drawing 11]



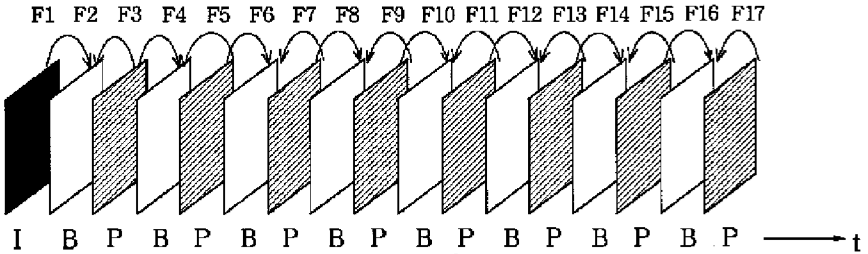
高能率符号化

## [Drawing 12]



グループオブピクチャ
F1 F2 F3 F4 F5 F6 F7 F8 F9 F10 F11 F12 F13 F14 F15 F16 F17
I B P B P B P B P B P B P B P B P
t

(A)前方向予測 P−ピクチャ

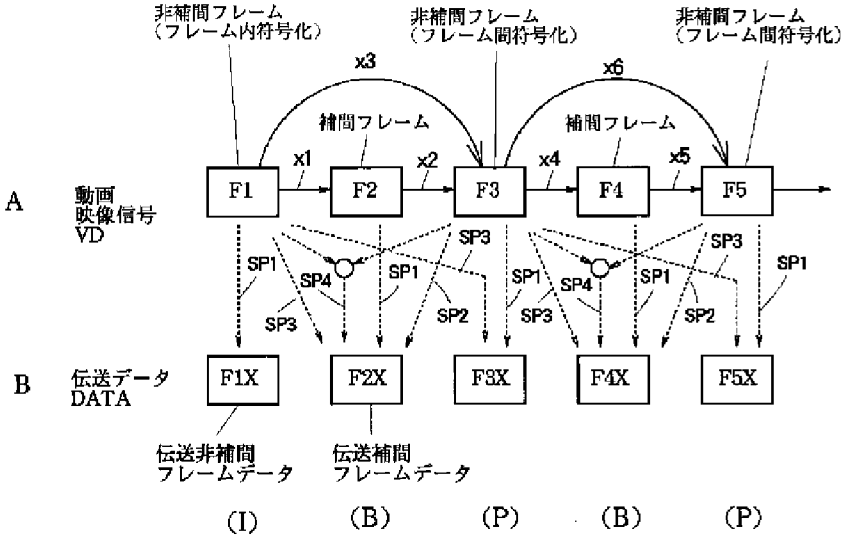


F1 F2 F3 F4 F5 F6 F7 F8 F9 F10 F11 F12 F13 F14 F15 F16 F17
I B P B P B P B P B P B P B P B P
t

(B)両方向予測 B−ピクチャ

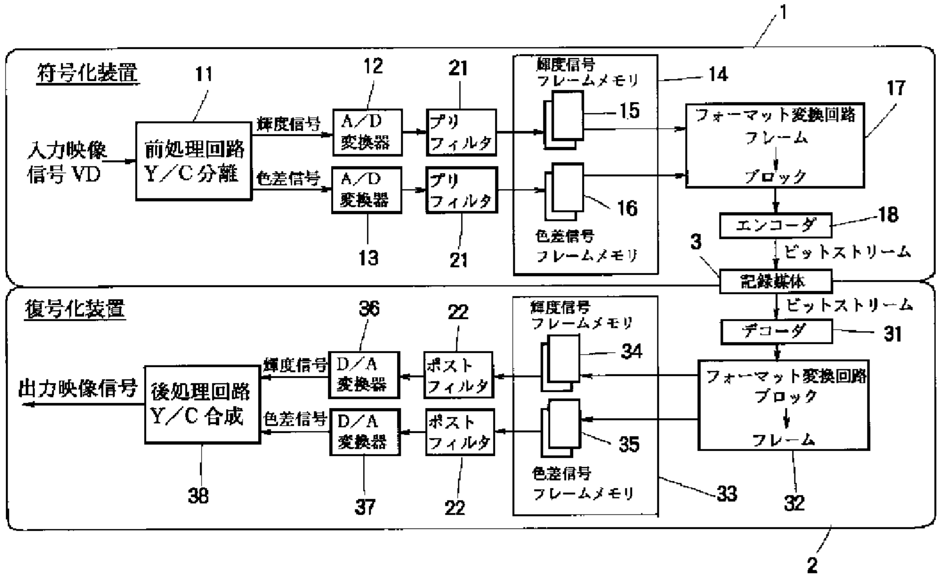
ピクチャタイプ I, P, B−picture

## [Drawing 13]



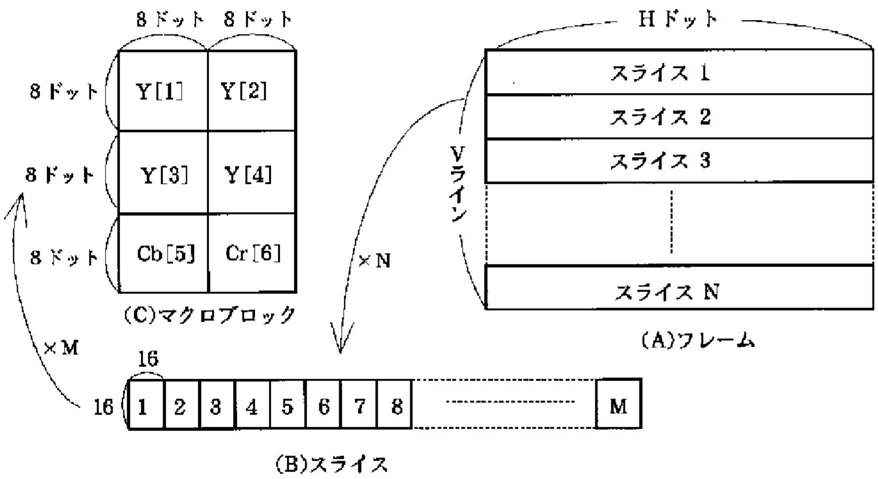
動画信号符号化方法の原理

## [Drawing 14]



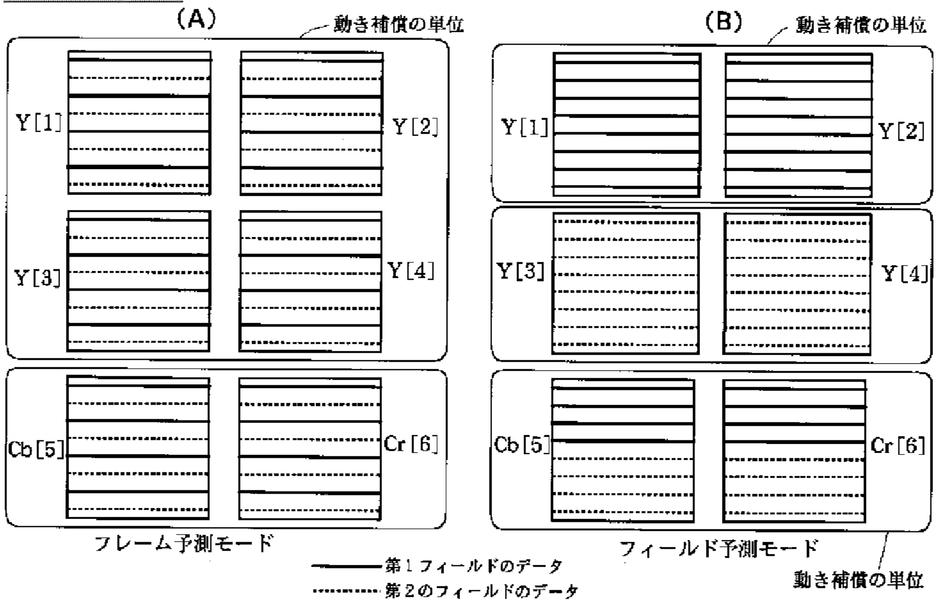
動画像符号化／復号化装置

## [Drawing 15]



画像データの構造

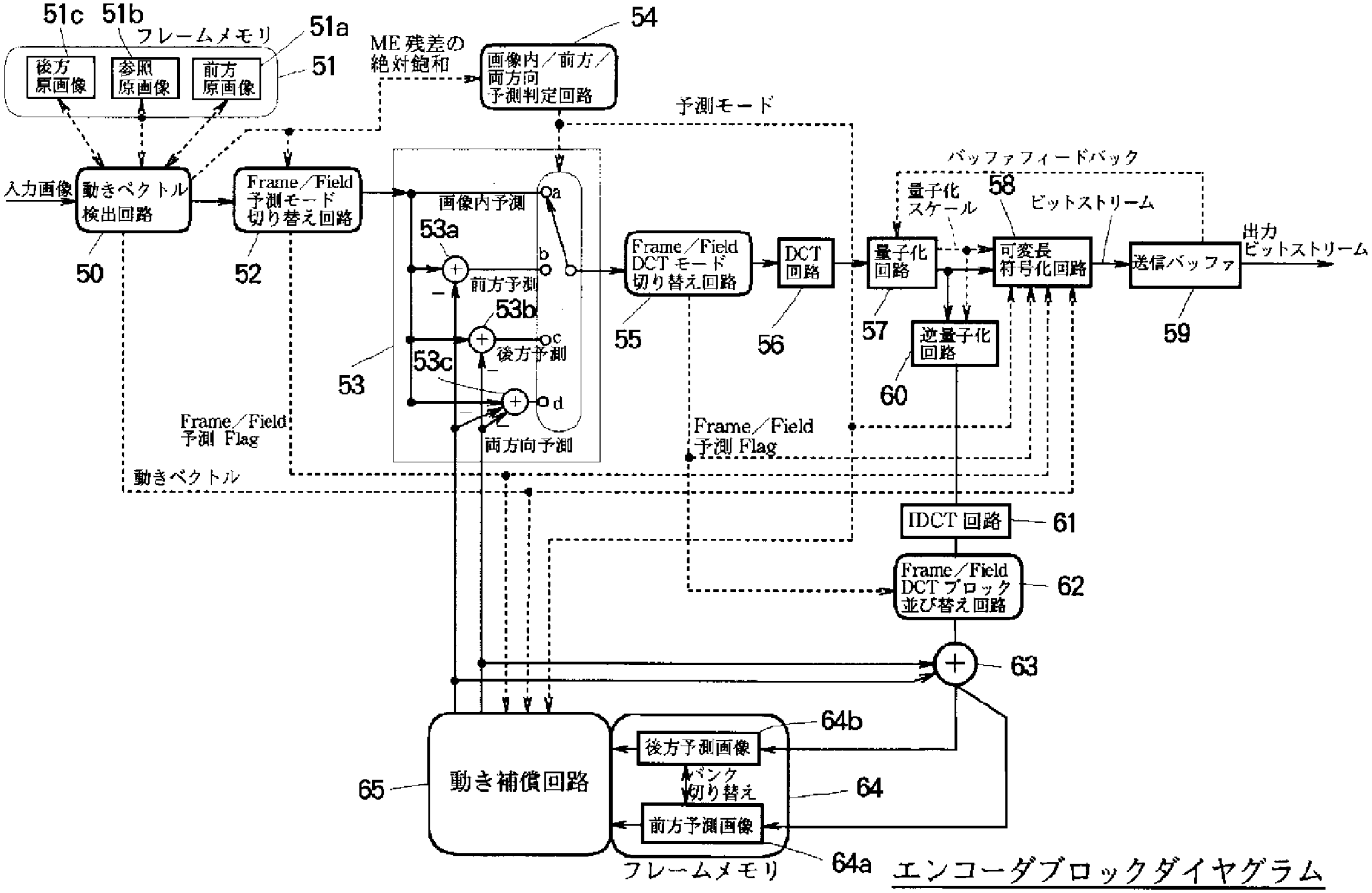
## [Drawing 17]

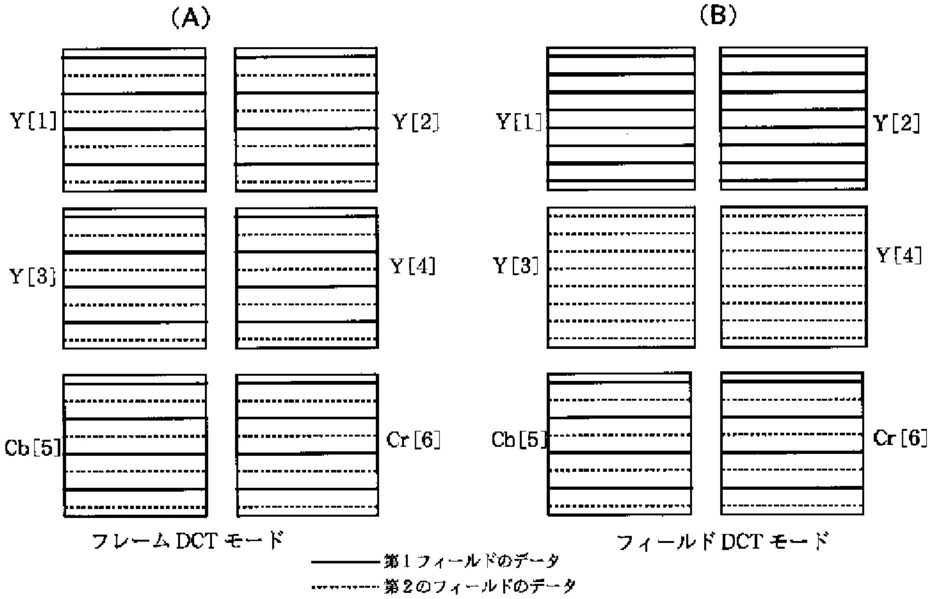


フレーム／フィールド予測モード

## [Drawing 16]

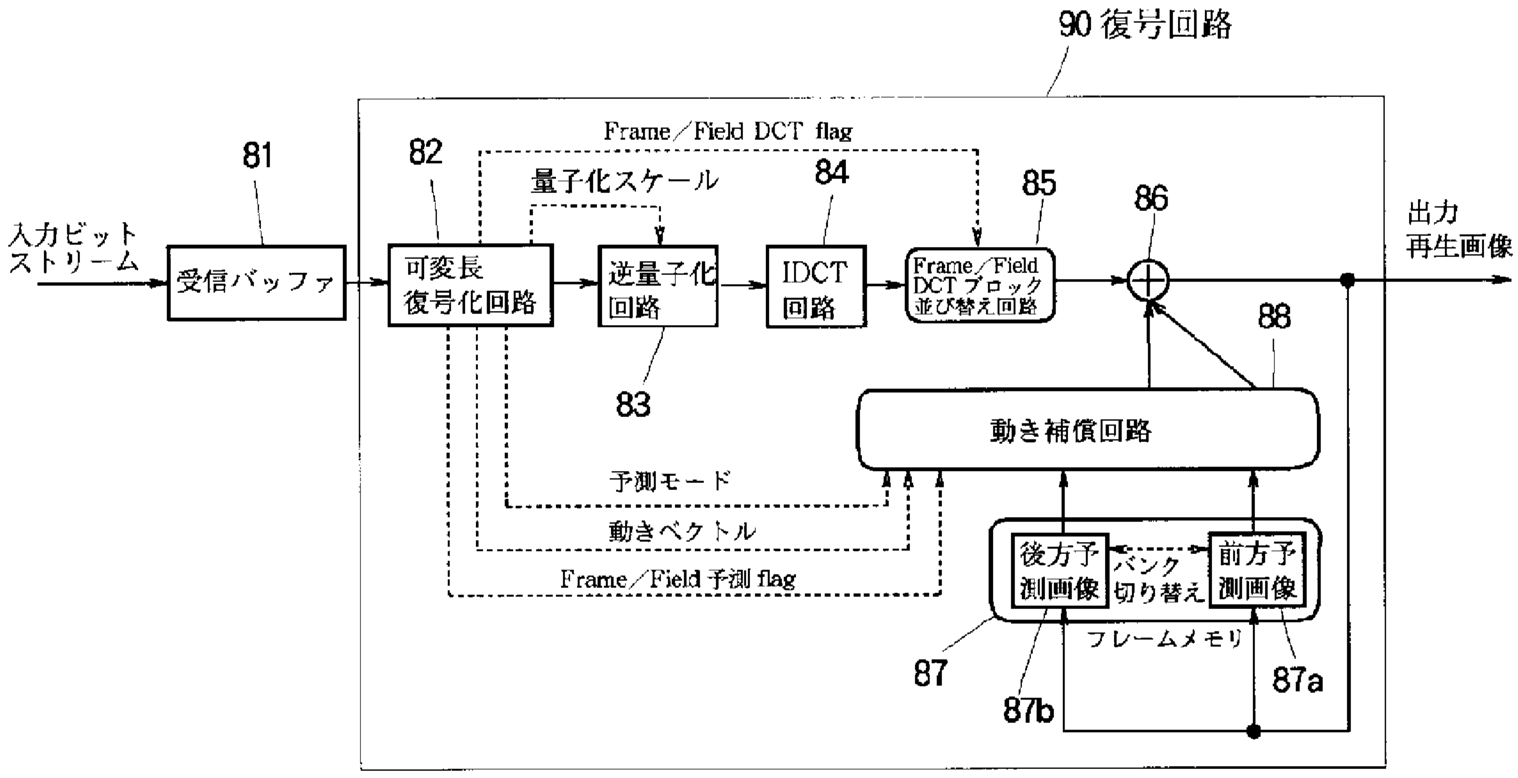
[Drawing 18]


51c
51b
フレームメモリ
51a
51
後方
原画像
参照
原画像
前方
原画像
ME 残差の
絶対飽和
54
画像内／前方／
両方向
予測判定回路
予測モード
入力画像
動きベクトル
検出回路
50
Frame／Field
予測モード
切り替え回路
52
画像内予測
a
53a
b
前方予測
53b
c
後方予測
53c
d
両方向予測
53
Frame／Field
予測 Flag
動きベクトル
Frame／Field
DCT モード
切り替え回路
55
DCT
回路
56
バッファフィードバック
量子化
スケール
58
ビットストリーム
量子化
回路
57
可変長
符号化回路
送信バッファ
59
出力
ビットストリーム
逆量子化
回路
60
Frame／Field
予測 Flag
IDCT 回路
61
Frame／Field
DCT ブロック
並び替え回路
62
63
64b
後方予測画像
バンク
切り替え
64
前方予測画像
64a
65
動き補償回路
フレームメモリ
エンコーダブロックダイヤグラム



フレーム／フィールドDCT モード

[Drawing 19]



デコーダブロックダイヤグラム

[Translation done.]

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| Ｈ０４Ｎ　7/32 | | | | |
| Ｇ０６Ｔ　9/00 | | | | |
| Ｈ０３Ｍ　7/30 | Ｚ | 8842－5Ｊ | | |
| | | | Ｈ０４Ｎ　7/ 137 | Ｚ |
| | | | Ｇ０６Ｆ　15/ 66　　３３０ | Ｄ |

審査請求　未請求　請求項の数８　ＯＬ　（全 27 頁）

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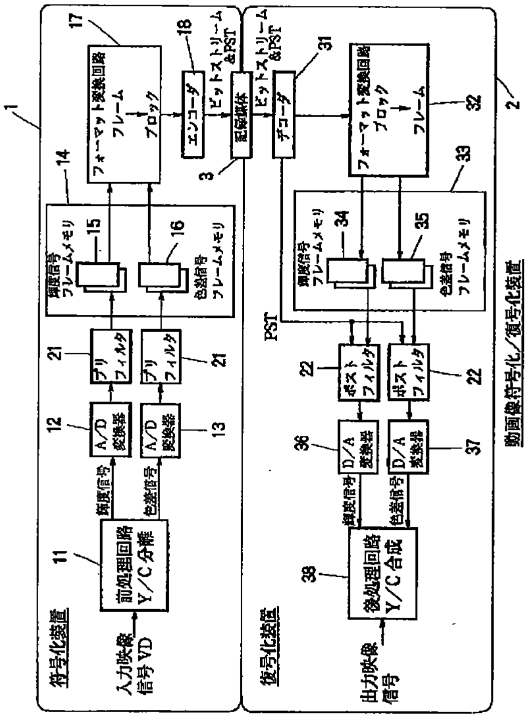
(74)代理人　弁理士　稲本　義雄

# (54)【発明の名称】　画像信号符号化装置及び画像信号復号化装置

(57)【要約】

【目的】　簡単な構成により復号化した画像信号を最適に補正する。

【構成】　符号化装置１のエンコーダ１８は、画像データであるビットストリームと同時にプリフィルタ２１の符号化条件を示すＰＳＴフラグを符号化し、ビットストリームと共にＰＳＴフラグを記録媒体３に伝送する。記録媒体３に符号化されて記憶されたビットストリームとＰＳＴフラグは、複合化装置２のデコーダ３１で複合化され、複合化されたビットストリームは、フォーマット変換回路３２に入力され、ブロックフォーマットからフレームフォーマットに変換される。一方、複合化されたＰＳＴフラグは、ポストフィルタ２２に伝送され、ポストフィルタ２２では、ＰＳＴフラグにより最適フィルタを選択するようになっている。



【特許請求の範囲】

【請求項１】　画像信号を所定の予測画像信号に基づいて符号化する符号化手段を備えた画像信号符号化装置において、
前記符号化手段は、前記予測画像信号に基づいて前記画像信号を符号化する際に、前記画像信号の符号化条件を示す符号化条件フラグを符号化することを特徴とする画像信号符号化装置。

【請求項２】　前記画像信号は、ビットストリームの画像情報であり、
前記符号化フラグは、ビットストリームの前記画像情報のユーザエリア中に存在することを特徴とする請求項１に記載の画像信号符号化装置。

【請求項３】　前記符号化手段が符号化するビットストリームの前記画像情報の符号化ビットレートに基づき、前記符号化フラグを設定するフラグ設定手段をさらに備えたことを特徴とする請求項２に記載の画像信号符号化装置。

【請求項４】　所定の予測画像信号に基づき画像信号を符号化した符号化画像信号を復号化する画像信号復号化装置において、
前記符号化画像信号は、前記画像信号及び前記画像信号の符号化条件を示す符号化条件フラグとからなり、
前記符号化条件フラグに基づいて、復号化された前記画像信号を補正する画像補正手段を具備したことを特徴とする画像信号復号化装置。

【請求項５】　前記画像信号は、ビットストリームの画像情報であり、
前記符号化フラグは、前記画像情報のユーザエリア中に存在することを特徴とする請求項４に記載の画像信号復号化装置。

【請求項６】　前記符号化フラグは、符号化されたビットストリームの前記画像情報の符号化ビットレートに基づき設定されることを特徴とする請求項５に記載の画像信号復号化装置。

【請求項７】　前記画像補正手段は、複数のフィルタからなり、前記フラグに基づいて複数の前記フィルタを選択して前記画像信号を補正することを特徴とする請求項４乃至６のいずれか１つに記載の画像信号復号化装置。

【請求項８】　前記フィルタは、メディアンフィルタであることを特徴とする請求項４乃至７のいずれか１つに記載の画像信号復号化装置。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、動画像データを圧縮して伝送する場合に用いて好適な画像信号符号化装置及び画像信号復号化装置に関する。

【０００２】

【従来の技術】動画像データを光磁気ディスクや磁気テープ等にデジタル的に記録する場合、あるいは所定の伝送媒体を介して伝送する場合、データを符号化し、圧縮して、データ量を減少するようにしている。

【０００３】例えば、テレビ会議システム、テレビ電話システムなどのように、動画像信号を遠隔地に伝送するシステムにおいては、伝送路を効率良く利用するため、映像信号のライン相関やフレーム間相関を利用して、画像信号を圧縮符号化するようになされている。

【０００４】ライン相関を利用すると、画像信号を、例えばＤＣＴ（離散コサイン変換）処理するなどして圧縮することができる。

【０００５】また、フレーム間相関を利用すると、画像信号をさらに圧縮して符号化することが可能となる。例えば図１１に示すように、時刻ｔ１，ｔ２，ｔ３において、フレーム画像ＰＣ１，ＰＣ２，ＰＣ３がそれぞれ発生しているとき、フレーム画像ＰＣ１とＰＣ２の画像信号の差を演算して、ＰＣ１２を生成し、また、フレーム画像ＰＣ２とＰＣ３の差を演算して、ＰＣ２３を生成する。通常、時間的に隣接するフレームの画像は、それ程大きな変化を有していないため、両者の差を演算すると、その差分信号は小さな値のものとなる。そこで、この差分信号を符号化すれば、符号量を圧縮することができる。

【０００６】しかしながら、差分信号のみを伝送したのでは、元の画像を復元することができない。そこで、各フレームの画像を、Ｉピクチャ、ＰピクチャまたはＢピクチャの３種類のピクチャのいずれかのピクチャとし、画像信号を圧縮符号化するようにしている。

【０００７】即ち、例えば図１２に示すように、フレームＦ１乃至Ｆ１７までの１７フレームの画像信号をグループオブピクチャ（ＧＯＰ）とし、処理の１単位とする。そして、その先頭のフレームＦ１の画像信号はＩピクチャとして符号化し、第２番目のフレームＦ２はＢピクチャとして、また第３番目のフレームＦ３はＰピクチャとして、それぞれ処理する。以下、第４番目以降のフレームＦ４乃至Ｆ１７は、ＢピクチャまたはＰピクチャとして交互に処理する。

【０００８】Ｉピクチャの画像信号としては、その１フレーム分の画像信号をそのまま伝送する。これに対して、Ｐピクチャの画像信号としては、基本的には、図１２（Ａ）に示すように、それより時間的に先行するＩピクチャまたはＰピクチャの画像信号からの差分を伝送する。さらにＢピクチャの画像信号としては、基本的には、図１２（Ｂ）に示すように、時間的に先行するフレームまたは後行するフレームの両方の平均値からの差分を求め、その差分を符号化する。

【０００９】図１３は、このようにして、動画像信号を符号化する方法の原理を示している。同図に示すように、最初のフレームＦ１は、Ｉピクチャとして処理されるため、そのまま伝送データＦ１Ｘとして伝送路に伝送される（画像内符号化）。これに対して、第２のフレー

ムＦ２は、Ｂピクチャとして処理されるため、時間的に先行するフレームＦ１と、時間的に後行するフレームＦ３の平均値との差分（予測誤差）が演算され、その差分が伝送データＦ２Ｘとして伝送される。

【００１０】但し、このＢピクチャとしての処理は、さらに細かく説明すると、４種類存在する。その第１の処理は、元のフレームＦ２のデータをそのまま伝送データＦ２Ｘとして伝送するものであり（ＳＰ１）（イントラ（画像内予測）符号化）、Ｉピクチャにおける場合と同様の処理となる。第２の処理は、時間的に後のフレームＦ３からの差分を演算し、その差分（ＳＰ２）を伝送するものである（後方予測符号化）。第３の処理は、時間的に先行するフレームＦ１との差分（ＳＰ３）を伝送するものである（前方予測符号化）。さらに第４の処理は、時間的に先行するフレームＦ１と後行するフレームＦ３の平均値との差分（ＳＰ４）を生成し、これを伝送データＦ２Ｘとして伝送するものである（両方向予測符号化）。

【００１１】この４つの方法のうち、伝送データが最も少なくなる方法が採用される。

【００１２】尚、差分データを伝送するとき、差分を演算する対象となるフレームの画像（予測画像）との間の動きベクトルｘ１（フレームＦ１とＦ２の間の動きベクトル）（前方予測の場合）、もしくはｘ２（フレームＦ３とＦ２の間の動きベクトル）（後方予測の場合）、またはｘ１とｘ２の両方（両方向予測の場合）が、差分データとともに伝送される。

【００１３】また、ＰピクチャのフレームＦ３は、時間的に先行するフレームＦ１を予測画像として、このフレームとの差分信号（ＳＰ３）と、動きベクトルｘ３が演算され、これが伝送データＦ３Ｘとして伝送される（前方予測符号化）。あるいはまた、元のフレームＦ３のデータが、そのままデータＦ３Ｘとして伝送される（ＳＰ１）（イントラ符号化）。いずれの方法により伝送されるかは、Ｂピクチャにおける場合と同様に、伝送データがより少なくなる方が選択される。

【００１４】図１４は、上述した原理に基づいて、動画像信号を符号化して伝送し、これを復号化する装置の構成例を示している。符号化装置１は、入力された映像信号を符号化し、伝送路としての記録媒体３に伝送するようになされている。そして、復号化装置２は、記録媒体３に記録された信号を再生し、これを復号して出力するようになされている。

【００１５】符号化装置１においては、入力された映像信号が前処理回路１１に入力され、そこで輝度信号と色信号（この実施例の場合、色差信号）が分離され、それぞれＡ／Ｄ変換器１２，１３でＡ／Ｄ変換される。Ａ／Ｄ変換器１２，１３によりＡ／Ｄ変換されてデジタル信号となった映像信号は、プリフィルタ２１によって処理された後フレームメモリ１４に供給され、記憶される。フレームメモリ１４は、輝度信号を輝度信号フレームメモリ１５に、また、色差信号を色差信号フレームメモリ１６に、それぞれ記憶させる。

【００１６】プリフィルタ２１は、符号化効率を向上させるための処理を行う。これは例えば、ノイズ除去フィルタであり、また例えば帯域を制限するためのフィルタである。

【００１７】フォーマット変換回路１７は、フレームメモリ１４に記憶されたフレームフォーマットの信号を、ブロックフォーマットの信号に変換する。即ち、図１５に示すように、フレームメモリ１４に記憶された映像信号は、１ライン当りＨドットのラインがＶライン集められたフレームフォーマットのデータとされている。フォーマット変換回路１７は、この１フレームの信号を、１６ラインを単位としてＮ個のスライスに区分する。そして、各スライスは、Ｍ個のマクロブロックに分割される。各マクロブロックは、１６×１６個の画素（ドット）に対応する輝度信号により構成され、この輝度信号は、さらに８×８ドットを単位とするブロックＹ［１］乃至Ｙ［４］に区分される。そして、この１６×１６ドットの輝度信号には、８×８ドットのＣｂ信号と、８×８ドットのＣｒ信号が対応される。

【００１８】このように、ブロックフォーマットに変換されたデータは、フォーマット変換回路１７からエンコーダ１８に供給され、ここでエンコード（符号化）が行われる。その詳細については、図１６を参照して後述する。

【００１９】エンコーダ１８によりエンコードされた信号は、ビットストリームとして伝送路に出力される。例えば記録回路１９に供給され、デジタル信号として記録媒体３に記録される。

【００２０】再生回路３０により記録媒体３より再生されたデータは、復号化装置２のデコーダ３１に供給され、デコードされる。デコーダ３１の詳細については、図１９を参照して後述する。

【００２１】デコーダ３１によりデコードされたデータは、フォーマット変換回路３２に入力され、ブロックフォーマットからフレームフォーマットに変換される。そして、フレームフォーマットの輝度信号は、フレームメモリ３３の輝度信号フレームメモリ３４に供給され、記憶され、色差信号は色差信号フレームメモリ３５に供給され、記憶される。輝度信号フレームメモリ３４と色差信号フレームメモリ３５より読み出された輝度信号と色差信号は、ポストフィルタ２２によって処理された後、Ｄ／Ａ変換器３６と３７によりそれぞれＤ／Ａ変換され、後処理回路３８に供給され、合成される。そして、例えば、図示せぬＣＲＴなどのディスプレイに出力され、表示される。

【００２２】ポストフィルタ２２は、画質を改善するための処理を行う。例えばブロック歪やモスキートノイズ

を除去するためのフィルタである。

【００２３】次に図１６を参照して、エンコーダ１８の構成例について説明する。

【００２４】符号化されるべき画像データは、マクロブロック単位で動きベクトル検出回路５０に入力される。動きベクトル検出回路５０は、予め設定された所定のシーケンスに従って、各フレームの画像データを、Ｉピクチャ、Ｐピクチャ、またはＢピクチャとして処理する。シーケンシャルに入力される各フレームの画像を、Ｉ，Ｐ，Ｂのいずれのピクチャとして処理するかは、予め定められている（例えば、図１５に示したように、フレームＦ１乃至Ｆ１７により構成されるグループオブピクチャが、Ｉ，Ｂ，Ｐ，Ｂ，Ｐ，・・・Ｂ，Ｐとして処理される）。

【００２５】Ｉピクチャとして処理されるフレーム（例えばフレームＦ１）の画像データは、動きベクトル検出回路５０からフレームメモリ５１の前方原画像部５１ａに転送、記憶され、Ｂピクチャとして処理されるフレーム（例えばフレームＦ２）の画像データは、参照原画像部５１ｂに転送、記憶され、Ｐピクチャとして処理されるフレーム（例えばフレームＦ３）の画像データは、後方原画像部５１ｃに転送、記憶される。

【００２６】また、次のタイミングにおいて、さらにＢピクチャ（フレームＦ４）またはＰピクチャ（フレームＦ５）として処理すべきフレームの画像が入力されたとき、それまで後方原画像部５１ｃに記憶されていた最初のＰピクチャ（フレームＦ３）の画像データが、前方原画像部５１ａに転送され、次のＢピクチャ（フレームＦ４）の画像データが、参照原画像部５１ｂに記憶（上書き）され、次のＰピクチャ（フレームＦ５）の画像データが、後方原画像部５１ｃに記憶（上書き）される。このような動作が順次繰り返される。

【００２７】フレームメモリ５１に記憶された各ピクチャの信号は、そこから読み出され、予測モード切り替え回路５２において、フレーム予測モード処理、またはフィールド予測モード処理が行なわれる。さらにまた、予測判定回路５４の制御の下に、演算部５３において、画像内予測、前方予測、後方予測、または両方向予測の演算が行なわれる。これらの処理のうち、いずれの処理を行なうかは、予測誤差信号（処理の対象とされている参照画像と、これに対する予測画像との差分）に対応して決定される。このため、動きベクトル検出回路５０は、この判定に用いられる予測誤差信号の絶対値和（自乗和でもよい）を生成する。

【００２８】ここで、予測モード切り替え回路５２におけるフレーム予測モードとフィールド予測モードについて説明する。

【００２９】フレーム予測モードが設定された場合においては、予測モード切り替え回路５２は、動きベクトル検出回路５０より供給される４個の輝度ブロックＹ［１］乃至Ｙ［４］を、そのまま後段の演算部５３に出力する。即ち、この場合においては、図８に示すように、各輝度ブロックに奇数フィールドのラインのデータと、偶数フィールドのラインのデータとが混在した状態となっている。このフレーム予測モードにおいては、４個の輝度ブロック（マクロブロック）を単位として予測が行われ、４個の輝度ブロックに対して１個の動きベクトルが対応される。

【００３０】これに対して、予測モード切り替え回路５２は、フィールド予測モードにおいては、図１７（A）に示す構成で動きベクトル検出回路５０より入力される信号を、図１７（B）に示すように、４個の輝度ブロックのうち、輝度ブロックＹ［１］とＹ［２］を、例えば奇数フィールドのラインのドットによりのみ構成させ、他の２個の輝度ブロックＹ［３］とＹ［４］を、偶数フィールドのラインのデータにより構成させて、演算部５３に出力する。この場合においては、２個の輝度ブロックＹ［１］とＹ［２］に対して、１個の動きベクトルが対応され、他の２個の輝度ブロックＹ［３］とＹ［４］に対して、他の１個の動きベクトルが対応される。

【００３１】動きベクトル検出回路５０は、フレーム予測モードにおける予測誤差の絶対値和と、フィールド予測モードにおける予測誤差の絶対値和を、予測モード切り替え回路５２に出力する。予測モード切り替え回路５２は、フレーム予測モードとフィールド予測モードにおける予測誤差の絶対値和を比較し、その値が小さい予測モードに対応する処理を施して、データを演算部５３に出力する。

【００３２】但し、このような処理は、実際には動きベクトル検出回路５０で行われる。即ち、動きベクトル検出回路５０は、決定されたモードに対応する構成の信号を予測モード切り替え回路５２に出力し、予測モード切り替え回路５２は、その信号を、そのまま後段の演算部５３に出力する。

【００３３】尚、色差信号は、フレーム予測モードの場合、図１７（A）に示すように、奇数フィールドのラインのデータと偶数フィールドのラインのデータとが混在する状態で、演算部５３に供給される。また、フィールド予測モードの場合、図１７（B）に示すように、各色差ブロックＣｂ，Ｃｒの上半分（４ライン）が、輝度ブロックＹ［１］，Ｙ［２］に対応する奇数フィールドの色差信号とされ、下半分（４ライン）が、輝度ブロックＹ［３］，Ｙ［４］に対応する偶数フィールドの色差信号とされる。

【００３４】また、動きベクトル検出回路５０は、次のようにして、予測判定回路５４において、画像内予測、前方予測、後方予測、または両方向予測のいずれの予測を行なうかを決定するための予測誤差の絶対値和を生成する。

【００３５】即ち、画像内予測の予測誤差の絶対値和と

して、参照画像のマクロブロックの信号Ａijの和ΣＡij の絶対値｜ΣＡij｜と、マクロブロックの信号Ａijの絶対値｜Ａij｜の和Σ｜Ａij｜の差を求める。また、前方予測の予測誤差の絶対値和として、参照画像のマクロブロックの信号Ａijと、予測画像のマクロブロックの信号Ｂijの差Ａij－Ｂijの絶対値｜Ａij－Ｂij｜の和Σ｜Ａij－Ｂij｜を求める。また、後方予測と両方向予測の予測誤差の絶対値和も、前方予測における場合と同様に（その予測画像を前方予測における場合と異なる予測画像に変更して）求める。

【００３６】これらの絶対値和は、予測判定回路５４に供給される。予測判定回路５４は、前方予測、後方予測および両方向予測の予測誤差の絶対値和のうち、最も小さいものを、インタ予測の予測誤差の絶対値和として選択する。さらに、このインタ予測の予測誤差の絶対値和と、画像内予測の予測誤差の絶対値和とを比較し、その小さい方を選択し、この選択した絶対値和に対応するモードを予測モードとして選択する。即ち、画像内予測の予測誤差の絶対値和の方が小さければ、画像内予測モードが設定される。インタ予測の予測誤差の絶対値和の方が小さければ、前方予測、後方予測または両方向予測モードのうち、対応する絶対値和が最も小さかったモードが設定される。

【００３７】このように、動きベクトル検出回路５０は、参照画像のマクロブロックの信号を、フレームまたはフィールド予測モードのうち、予測モード切り替え回路５２により選択されたモードに対応する構成で、予測モード切り替え回路５２を介して演算部５３に供給するとともに、４つの予測モードのうち、予測判定回路５４により選択された予測モードに対応する予測画像と参照画像の間の動きベクトルを検出し、可変長符号化回路５８と動き補償回路６５に出力する。上述したように、この動きベクトルとしては、対応する予測誤差の絶対値和が最小となるものが選択される。

【００３８】予測判定回路５４は、動きベクトル検出回路５０が前方原画像部５１ａよりＩピクチャの画像データを読み出しているとき、予測モードとして、フレームまたはフィールド（画像）内予測モード（動き補償を行わないモード）を設定し、演算部５３のスイッチ５３ｄを接点ａ側に切り替える。これにより、Ｉピクチャの画像データがＤＣＴモード切り替え回路５５に入力される。

【００３９】このＤＣＴモード切り替え回路５５は、図１８（Ａ）または図１８（Ｂ）に示すように、４個の輝度ブロックのデータを、奇数フィールドのラインと偶数フィールドのラインが混在する状態（フレームＤＣＴモード）、または、分離された状態（フィールドＤＣＴモード）、のいずれかの状態にして、ＤＣＴ回路５６に出力する。

【００４０】即ち、ＤＣＴモード切り替え回路５５は、奇数フィールドと偶数フィールドのデータを混在してＤＣＴ処理した場合における符号化効率と、分離した状態においてＤＣＴ処理した場合の符号化効率とを比較し、符号化効率の良好なモードを選択する。

【００４１】例えば、入力された信号を、図１８（Ａ）に示すように、奇数フィールドと偶数フィールドのラインが混在する構成とし、上下に隣接する奇数フィールドのラインの信号と偶数フィールドのラインの信号の差を演算し、さらにその絶対値の和（または自乗和）を求める。また、入力された信号を、図１８（Ｂ）に示すように、奇数フィールドと偶数フィールドのラインが分離した構成とし、上下に隣接する奇数フィールドのライン同士の信号の差と、偶数フィールドのライン同士の信号の差を演算し、それぞれの絶対値の和（または自乗和）を求める。さらに、両者（絶対値和）を比較し、小さい値に対応するＤＣＴモードを設定する。即ち、前者の方が小さければ、フレームＤＣＴモードを設定し、後者の方が小さければ、フィールドＤＣＴモードを設定する。

【００４２】そして、選択したＤＣＴモードに対応する構成のデータをＤＣＴ回路５６に出力するとともに、選択したＤＣＴモードを示すＤＣＴフラグを、可変長符号化回路５８、ＤＣＴブロック並び替え回路６２、および動き補償回路６５に出力する。

【００４３】予測モード切り替え回路５２における予測モード（図１７）と、このＤＣＴモード切り替え回路５５におけるＤＣＴモード（図１８）を比較して明らかなように、輝度ブロックに関しては、両者の各モードにおけるデータ構造は実質的に同一である。

【００４４】予測モード切り替え回路５２において、フレーム予測モード（奇数ラインと偶数ラインが混在するモード）が選択された場合、ＤＣＴモード切り替え回路５５においても、フレームＤＣＴモード（奇数ラインと偶数ラインが混在するモード）が選択される可能性が高く、また予測モード切り替え回路５２において、フィールド予測モード（奇数フィールドと偶数フィールドのデータが分離されたモード）が選択された場合、ＤＣＴモード切り替え回路５５において、フィールドＤＣＴモード（奇数フィールドと偶数フィールドのデータが分離されたモード）が選択される可能性が高い。

【００４５】しかしながら、必ずしも常にそのようになされるわけではなく、予測モード切り替え回路５２においては、予測誤差の絶対値和が小さくなるようにモードが決定され、ＤＣＴモード切り替え回路５５においては、符号化効率が良好となるようにモードが決定される。

【００４６】ＤＣＴモード切り替え回路５５より出力されたＩピクチャの画像データは、ＤＣＴ回路５６に入力され、ＤＣＴ（離散コサイン変換）処理され、ＤＣＴ係数に変換される。このＤＣＴ係数は、量子化回路５７に入力され、送信バッファ５９のデータ蓄積量（バッファ

蓄積量）に対応した量子化ステップで量子化された後、可変長符号化回路５８に入力される。

【００４７】可変長符号化回路５８は、量子化回路５７より供給される量子化ステップ（スケール）に対応して、量子化回路５７より供給される画像データ（いまの場合、Ｉピクチャのデータ）を、例えばハフマン符号などの可変長符号に変換し、送信バッファ５９に出力する。

【００４８】可変長符号化回路５８にはまた、量子化回路５７より量子化ステップ（スケール）、予測判定回路５４より予測モード（画像内予測、前方予測、後方予測、または両方向予測のいずれが設定されたかを示すモード）、動きベクトル検出回路５０より動きベクトル、予測モード切り替え回路５２より予測フラグ（フレーム予測モードまたはフィールド予測モードのいずれが設定されたかを示すフラグ）、およびＤＣＴモード切り替え回路５５が出力するＤＣＴフラグ（フレームＤＣＴモードまたはフィールドＤＣＴモードのいずれが設定されたかを示すフラグ）が入力されており、これらも可変長符号化される。

【００４９】送信バッファ５９は、入力されたデータを一時蓄積し、蓄積量に対応するデータを量子化回路５７に出力する。送信バッファ５９は、そのデータ残量が許容上限値まで増量すると、量子化制御信号によって量子化回路５７の量子化スケールを大きくすることにより、量子化データのデータ量を低下させる。また、これとは逆に、データ残量が許容下限値まで減少すると、送信バッファ５９は、量子化制御信号によって量子化回路５７の量子化スケールを小さくすることにより、量子化データのデータ量を増大させる。このようにして、送信バッファ５９のオーバフローまたはアンダフローが防止される。

【００５０】そして、送信バッファ５９に蓄積されたデータは、所定のタイミングで読み出され、伝送路に出力され、例えば記録媒体３に記録される。

【００５１】一方、量子化回路５７より出力されたＩピクチャのデータは、逆量子化回路６０に入力され、量子化回路５７より供給される量子化ステップに対応して逆量子化される。逆量子化回路６０の出力は、ＩＤＣＴ（逆ＤＣＴ）回路６１に入力され、逆ＤＣＴ処理された後、ＤＣＴブロック並び替え回路６２に入力される。ＤＣＴブロック並び替え回路６２は、入力されたデータを、予測モード切り替え回路５２から供給される予測フラグと、ＤＣＴモード切り替え回路５５から供給されるＤＣＴフラグに対応して、データの並び替えを行う。

【００５２】即ち、予測モード切り替え回路５２において、フレーム予測モードが設定されている場合、動き補償回路６５から読み出され、演算部５３に供給されるデータは、奇数フィールドのデータと偶数フィールドのデータとが混在する状態となされている。このデータが演算器６３にも供給される。このため、ＤＣＴブロック並び替え回路６２は、ＩＤＣＴ回路６１より供給されるデータを、フレームＤＣＴモードが設定されている場合、そのまま演算器６３に供給し、フィールドＤＣＴモードが設定されている場合、奇数フィールドのデータと偶数フィールドのデータとが分離された状態となされているため、これらが混在する状態にデータを並べ替えて、演算器６３に出力する。

【００５３】一方、予測モード切り替え回路５２において、フィールド予測モードが設定されている場合、動き補償回路６５より演算部５３に供給されるデータは、奇数フィールドのデータと偶数フィールドのデータとが分離した状態となされている。このため、ＤＣＴブロック並び替え回路５８は、ＤＣＴモード切り替え回路５５によりフィールドＤＣＴモードが設定されている場合、ＩＤＣＴ回路６１より出力されるデータをそのまま演算器６３に供給するが、フレームＤＣＴモードが設定されている場合、奇数フィールドのデータと偶数フィールドのデータとが混在する状態となされているため、これを、それぞれが分離された状態に並べ替えて、演算器６３に出力する。

【００５４】即ち、ＤＣＴブロック並び替え回路５８は、動き補償回路６５から演算部５３に供給されるデータの配列状態と同一の配列状態になるように、ＩＤＣＴ回路６１の出力するデータの並び替えを実行する。

【００５５】いまの場合、ＩＤＣＴ回路６１より出力されるデータは、Ｉピクチャのデータであるから、画像内予測とされている。このため、ＤＣＴモード切り替え回路５５がフレームＤＣＴフラグを出力しているとき、ＩＤＣＴ回路６１より出力されたデータは、そのまま演算器６３を介してフレームメモリ６５の前方予測画像部６５ａに供給され、記憶される。また、フィールドＤＣＴフラグが出力されているとき、データの並び替えが行われた後、記憶される。

【００５６】動きベクトル検出回路５０は、シーケンシャルに入力される各フレームの画像データを、たとえば、Ｉ，Ｂ，Ｐ，Ｂ，Ｐ，Ｂ・・・のピクチャとしてそれぞれ処理する場合、最初に入力されたフレームの画像データをＩピクチャとして処理した後、次に入力されたフレームの画像をＢピクチャとして処理する前に、さらにその次に入力されたフレームの画像データをＰピクチャとして処理する。Ｂピクチャは、後方予測を伴うため、後方予測画像としてのＰピクチャが先に用意されていないと、復号することができないからである。

【００５７】そこで動きベクトル検出回路５０は、Ｉピクチャの処理の次に、後方原画像部５１ｃに記憶されているＰピクチャの画像データの処理を開始する。そして、上述した場合と同様に、マクロブロック単位でのフレーム間差分（予測誤差）の絶対値和が、動きベクトル検出回路５０から予測モード切り替え回路５２と予測判

定回路５４に供給される。予測モード切り替え回路５２と予測判定回路５４は、このＰピクチャのマクロブロックの予測誤差の絶対値和に対応して、フレーム／フィールド予測モード、または画像内予測、前方予測、後方予測、もしくは両方向予測の予測モードを設定する。

【００５８】演算部５３は、画像内予測モードが設定されたとき、スイッチ５３ｄを上述したように接点ａ側に切り替える。従って、このデータは、Ｉピクチャのデータと同様に、ＤＣＴモード切り替え回路５５、ＤＣＴ回路５６、量子化回路５７、可変長符号化回路５８、送信バッファ５９を介して伝送路に伝送される。また、このデータは、逆量子化回路６０、ＩＤＣＴ回路６１、ＤＣＴブロック並び替え回路６２、演算器６３を介してフレームメモリ６４の後方予測画像部６４ｂに供給され、記憶される。

【００５９】前方予測モードの時、スイッチ５３ｄが接点ｂに切り替えられるとともに、フレームメモリ６４の前方予測画像部６４ａに記憶されている画像（いまの場合、Ｉピクチャの画像）データが読み出され、動き補償回路６５により、動きベクトル検出回路５０が出力する動きベクトルに対応して動き補償される。即ち、動き補償回路６５は、予測判定回路５４より前方予測モードの設定が指令されたとき、前方予測画像部６４ａの読み出しアドレスを、動きベクトル検出回路５０がいま出力しているマクロブロックの位置に対応する位置から動きベクトルに対応する分だけずらしてデータを読み出し、予測画像データを生成する。

【００６０】動き補償回路６５より出力された予測画像データは、演算器５３ａに供給される。演算器５３ａは、予測モード切り替え回路５２より供給された参照画像のマクロブロックのデータから、動き補償回路６５より供給された、このマクロブロックに対応する予測画像データを減算し、その差分（予測誤差）を出力する。この差分データは、ＤＣＴモード切り替え回路５５、ＤＣＴ回路５６、量子化回路５７、可変長符号化回路５８、送信バッファ５９を介して伝送路に伝送される。また、この差分データは、逆量子化回路６０、ＩＤＣＴ回路６１、ＤＣＴブロック並び替え回路６２により局所的に復号され、演算器６３に入力される。

【００６１】この演算器６３にはまた、演算器５３ａに供給されている予測画像データと同一のデータが供給されている。演算器６３は、ＤＣＴブロック並び替え回路６２が出力する差分データに、動き補償回路６５が出力する予測画像データを加算する。これにより、元の（復号した）Ｐピクチャの画像データが得られる。このＰピクチャの画像データは、フレームメモリ６４の後方予測画像部６４ｂに供給され、記憶される。

【００６２】動きベクトル検出回路５０は、このように、ＩピクチャとＰピクチャのデータが前方予測画像部６４ａと後方予測画像部６４ｂにそれぞれ記憶された

後、次にＢピクチャの処理を実行する。予測モード切り替え回路５２と予測判定回路５４は、マクロブロック単位でのフレーム間差分の絶対値和の大きさに対応して、フレーム／フィールドモードを設定し、また、予測モードを画像内予測モード、前方予測モード、後方予測モード、または両方向予測モードのいずれかに設定する。

【００６３】上述したように、画像内予測モードまたは前方予測モードの時、スイッチ５３ｄは接点ａまたはｂに切り替えられる。このとき、Ｐピクチャにおける場合と同様の処理が行われ、データが伝送される。

【００６４】これに対して、後方予測モードまたは両方向予測モードが設定された時、スイッチ５３ｄは、接点ｃまたはｄにそれぞれ切り替えられる。

【００６５】スイッチ５３ｄが接点ｃに切り替えられている後方予測モードの時、後方予測画像部６４ｂに記憶されている画像（いまの場合、Ｐピクチャの画像）データが読み出され、動き補償回路６５により、動きベクトル検出回路５０が出力する動きベクトルに対応して動き補償される。即ち、動き補償回路６５は、予測判定回路５４より後方予測モードの設定が指令されたとき、後方予測画像部６４ｂの読み出しアドレスを、動きベクトル検出回路５０がいま出力しているマクロブロックの位置に対応する位置から動きベクトルに対応する分だけずらしてデータを読み出し、予測画像データを生成する。

【００６６】動き補償回路６５より出力された予測画像データは、演算器５３ｂに供給される。演算器５３ｂは、予測モード切り替え回路５２より供給された参照画像のマクロブロックのデータから、動き補償回路６５より供給された予測画像データを減算し、その差分を出力する。この差分データは、ＤＣＴモード切り替え回路５５、ＤＣＴ回路５６、量子化回路５７、可変長符号化回路５８、送信バッファ５９を介して伝送路に伝送される。

【００６７】スイッチ５３ｄが接点ｄに切り替えられている両方向予測モードの時、前方予測画像部６４ａに記憶されている画像（いまの場合、Ｉピクチャの画像）データと、後方予測画像部６４ｂに記憶されている画像（いまの場合、Ｐピクチャの画像）データが読み出され、動き補償回路６５により、動きベクトル検出回路５０が出力する動きベクトルに対応して動き補償される。即ち、動き補償回路６５は、予測判定回路５４より両方向予測モードの設定が指令されたとき、前方予測画像部６４ａと後方予測画像部６４ｂの読み出しアドレスを、動きベクトル検出回路５０がいま出力しているマクロブロックの位置に対応する位置から動きベクトル（この場合の動きベクトルは、前方予測画像用と後方予測画像用の２つとなる）に対応する分だけずらしてデータを読み出し、予測画像データを生成する。

【００６８】動き補償回路６５より出力された予測画像データは、演算器５３ｃに供給される。演算器５３ｃ

は、動きベクトル検出回路５０より供給された参照画像のマクロブロックのデータから、動き補償回路６５より供給された予測画像データの平均値を減算し、その差分を出力する。この差分データは、ＤＣＴモード切り替え回路５５、ＤＣＴ回路５６、量子化回路５７、可変長符号化回路５８、送信バッファ５９を介して伝送路に伝送される。

【００６９】Ｂピクチャの画像は、他の画像の予測画像とされることがないため、フレームメモリ６４には記憶されない。

【００７０】尚、フレームメモリ６４において、前方予測画像部６４ａと後方予測画像部６４ｂは、必要に応じてバンク切り替えが行われ、所定の参照画像に対して、一方または他方に記憶されているものを、前方予測画像あるいは後方予測画像として切り替えて出力することができる。

【００７１】以上においては、輝度ブロックを中心として説明をしたが、色差ブロックについても図１５に示したマクロブロックと同様なマクロブロックを単位として処理され、伝送される。尚、色差ブロックを処理する場合の動きベクトルは、対応する輝度ブロックの動きベクトルを垂直方向と水平方向に、それぞれ１／２にしたものが用いられる。

【００７２】図１９は、図１４のデコーダ３１の一実施例である復号回路９０の構成を示すブロック図である。伝送路（記録媒体３）を介して伝送された符号化された画像データは、図示せぬ受信回路で受信されたり、再生回路で再生され、受信バッファ８１に一時記憶された後、復号回路９０の可変長復号化回路８２に供給される。可変長復号化回路８２は、受信バッファ８１より供給されたデータを可変長復号化し、動きベクトル、予測モード、予測フラグおよびＤＣＴフラグを動き補償回路８８に、また、量子化ステップ（スケール）を逆量子化回路８３に、それぞれ出力するとともに、復号された画像データを逆量子化回路８３に出力する。さらに、ＤＣＴフラグと予測フラグを、逆量子化回路８３に出力する。

【００７３】逆量子化回路８３は、可変長復号化回路８２より供給された画像データを、同じく可変長復号化回路８２より供給された量子化ステップに従って逆量子化し、ＩＤＣＴ回路８４に出力する。逆量子化回路８３より出力されたデータ（ＤＣＴ係数）は、ＩＤＣＴ回路８４で、逆ＤＣＴ処理され、元の画像データに戻される。

【００７４】この画像データは、さらにＤＣＴブロック並び替え回路８６に入力される。ＤＣＴブロック並び替え回路８６は、ＤＣＴフラグと予測フラグに対応して、このデータを、動き補償回路８８が演算部８７に出力するデータと同一の配列状態になるように並び替えを行い、演算器８７に出力する。

【００７５】ＤＣＴブロック並び替え回路８６より供給された画像データが、Ｉピクチャのデータである場合、そのデータは演算器８６より出力され、演算器８６に後に入力される画像データ（ＰピクチャまたはＢピクチャのデータ）の予測画像データ生成のために、フレームメモリ８７の前方予測画像部８７ａに供給されて記憶される。また、このデータは、フォーマット変換回路３２（図１４）に出力される。

【００７６】ＩＤＣＴ回路８４より供給された画像データが、その１フレーム前の画像データを予測画像データとするＰピクチャのデータであって、前方予測モードのデータである場合、フレームメモリ８７の前方予測画像部８７ａに記憶されている、１フレーム前の画像データ（Ｉピクチャのデータ）が読み出され、動き補償回路８８で可変長復号化回路８２より出力された動きベクトルに対応する動き補償が施される。そして、演算器８６において、ＤＣＴブロック並べ替え回路８６より供給された画像データ（差分のデータ）と加算され、出力される。この加算されたデータ、即ち、復号されたＰピクチャのデータは、演算器８６に後に入力される画像データ（ＢピクチャまたはＰピクチャのデータ）の予測画像データ生成のために、フレームメモリ８７の後方予測画像部８７ｂに供給されて記憶される。

【００７７】Ｐピクチャのデータであっても、画像内予測モードのデータは、Ｉピクチャのデータと同様に、演算器８７で特に処理は行わず、そのまま後方予測画像部８７ｂに記憶される。

【００７８】このＰピクチャは、次のＢピクチャの次に表示されるべき画像であるため、この時点では、まだフォーマット変換回路３２へ出力されない（上述したように、Ｂピクチャの後に入力されたＰピクチャが、Ｂピクチャより先に処理され、伝送されている）。

【００７９】ＤＣＴブロック並べ替え回路８６より供給された画像データが、Ｂピクチャのデータである場合、可変長復号化回路８２より供給された予測モードに対応して、フレームメモリ８７の前方予測画像部８７ａに記憶されているＩピクチャの画像データ（前方予測モードの場合）、後方予測画像部８７ｂに記憶されているＰピクチャの画像データ（後方予測モードの場合）、または、その両方の画像データ（両方向予測モードの場合）が読み出され、動き補償回路８８において、可変長復号化回路８２より出力された動きベクトルに対応する動き補償が施されて、予測画像が生成される。但し、動き補償を必要としない場合（画像内予測モードの場合）、予測画像は生成されない。

【００８０】このようにして、動き補償回路８８で動き補償が施されたデータは、演算器８６において、ＤＣＴブロック並べ替え回路８６出力と加算される。この加算出力は、フォーマット変換回路３２に出力される。

【００８１】但し、この加算出力はＢピクチャのデータであり、他の画像の予測画像生成のために利用されるこ

定回路５４に供給される。予測モード切り替え回路５２と予測判定回路５４は、このＰピクチャのマクロブロックの予測誤差の絶対値和に対応して、フレーム／フィールド予測モード、または画像内予測、前方予測、後方予測、もしくは両方向予測の予測モードを設定する。

【００５８】演算部５３は、画像内予測モードが設定されたとき、スイッチ５３ｄを上述したように接点ａ側に切り替える。従って、このデータは、Ｉピクチャのデータと同様に、ＤＣＴモード切り替え回路５５、ＤＣＴ回路５６、量子化回路５７、可変長符号化回路５８、送信バッファ５９を介して伝送路に伝送される。また、このデータは、逆量子化回路６０、ＩＤＣＴ回路６１、ＤＣＴブロック並び替え回路６２、演算器６３を介してフレームメモリ６４の後方予測画像部６４ｂに供給され、記憶される。

【００５９】前方予測モードの時、スイッチ５３ｄが接点ｂに切り替えられるとともに、フレームメモリ６４の前方予測画像部６４ａに記憶されている画像（いまの場合、Ｉピクチャの画像）データが読み出され、動き補償回路６５により、動きベクトル検出回路５０が出力する動きベクトルに対応して動き補償される。即ち、動き補償回路６５は、予測判定回路５４より前方予測モードの設定が指令されたとき、前方予測画像部６４ａの読み出しアドレスを、動きベクトル検出回路５０がいま出力しているマクロブロックの位置に対応する位置から動きベクトルに対応する分だけずらしてデータを読み出し、予測画像データを生成する。

【００６０】動き補償回路６５より出力された予測画像データは、演算器５３ａに供給される。演算器５３ａは、予測モード切り替え回路５２より供給された参照画像のマクロブロックのデータから、動き補償回路６５より供給された、このマクロブロックに対応する予測画像データを減算し、その差分（予測誤差）を出力する。この差分データは、ＤＣＴモード切り替え回路５５、ＤＣＴ回路５６、量子化回路５７、可変長符号化回路５８、送信バッファ５９を介して伝送路に伝送される。また、この差分データは、逆量子化回路６０、ＩＤＣＴ回路６１、ＤＣＴブロック並び替え回路６２により局所的に復号され、演算器６３に入力される。

【００６１】この演算器６３にはまた、演算器５３ａに供給されている予測画像データと同一のデータが供給されている。演算器６３は、ＤＣＴブロック並び替え回路６２が出力する差分データに、動き補償回路６５が出力する予測画像データを加算する。これにより、元の（復号した）Ｐピクチャの画像データが得られる。このＰピクチャの画像データは、フレームメモリ６４の後方予測画像部６４ｂに供給され、記憶される。

【００６２】動きベクトル検出回路５０は、このように、ＩピクチャとＰピクチャのデータが前方予測画像部６４ａと後方予測画像部６４ｂにそれぞれ記憶された後、次にＢピクチャの処理を実行する。予測モード切り替え回路５２と予測判定回路５４は、マクロブロック単位でのフレーム間差分の絶対値和の大きさに対応して、フレーム／フィールドモードを設定し、また、予測モードを画像内予測モード、前方予測モード、後方予測モード、または両方向予測モードのいずれかに設定する。

【００６３】上述したように、画像内予測モードまたは前方予測モードの時、スイッチ５３ｄは接点ａまたはｂに切り替えられる。このとき、Ｐピクチャにおける場合と同様の処理が行われ、データが伝送される。

【００６４】これに対して、後方予測モードまたは両方向予測モードが設定された時、スイッチ５３ｄは、接点ｃまたはｄにそれぞれ切り替えられる。

【００６５】スイッチ５３ｄが接点ｃに切り替えられている後方予測モードの時、後方予測画像部６４ｂに記憶されている画像（いまの場合、Ｐピクチャの画像）データが読み出され、動き補償回路６５により、動きベクトル検出回路５０が出力する動きベクトルに対応して動き補償される。即ち、動き補償回路６５は、予測判定回路５４より後方予測モードの設定が指令されたとき、後方予測画像部６４ｂの読み出しアドレスを、動きベクトル検出回路５０がいま出力しているマクロブロックの位置に対応する位置から動きベクトルに対応する分だけずらしてデータを読み出し、予測画像データを生成する。

【００６６】動き補償回路６５より出力された予測画像データは、演算器５３ｂに供給される。演算器５３ｂは、予測モード切り替え回路５２より供給された参照画像のマクロブロックのデータから、動き補償回路６５より供給された予測画像データを減算し、その差分を出力する。この差分データは、ＤＣＴモード切り替え回路５５、ＤＣＴ回路５６、量子化回路５７、可変長符号化回路５８、送信バッファ５９を介して伝送路に伝送される。

【００６７】スイッチ５３ｄが接点ｄに切り替えられている両方向予測モードの時、前方予測画像部６４ａに記憶されている画像（いまの場合、Ｉピクチャの画像）データと、後方予測画像部６４ｂに記憶されている画像（いまの場合、Ｐピクチャの画像）データが読み出され、動き補償回路６５により、動きベクトル検出回路５０が出力する動きベクトルに対応して動き補償される。即ち、動き補償回路６５は、予測判定回路５４より両方向予測モードの設定が指令されたとき、前方予測画像部６４ａと後方予測画像部６４ｂの読み出しアドレスを、動きベクトル検出回路５０がいま出力しているマクロブロックの位置に対応する位置から動きベクトル（この場合の動きベクトルは、前方予測画像用と後方予測画像用の２つとなる）に対応する分だけずらしてデータを読み出し、予測画像データを生成する。

【００６８】動き補償回路６５より出力された予測画像データは、演算器５３ｃに供給される。演算器５３ｃ

は、フォーマット変換回路３２に入力され、ブロックフォーマットからフレームフォーマットに変換される。一方、復号化されたＰＳＴフラグは、ポストフィルタ２２に伝送され、ポストフィルタ２２では、ＰＳＴフラグにより最適フィルタを選択するようになっている。

【００９９】エンコーダ１８によるＰＳＴフラグの決定は、本実施例では次に示すような方法によりなされる。即ち、外部から強制的にＰＳＴフラグを入力し設定する方法であり、このＰＳＴフラグの決定方法について説明する。

【０１００】この決定方法を実現するエンコーダ１８の構成を図２に示す。入力されたＰＳＴフラグは、可変長符号化回路５８に入力される。そして可変長符号化回路５８では、従来例と同様にビットストリームを可変長符号化すると共に、入力されたＰＳＴフラグを可変長符号化する。

【０１０１】そして、ＰＳＴフラグは、ビットストリーム中のユーザデータ（user data）としてビットストリームと共に記憶媒体３に記憶される。ＭＰＥＧ，ＭＰＥＧ２方式では、"user data"は、シーケンス、ＧＯＰ、ピクチャヘッダの後に設定可能であるので、ＰＳＴフラグは同様に、シーケンス、ＧＯＰ、ピクチャヘッダ単位で設定可能である。

【０１０２】ここで、表１乃至表４にＭＰＥＧ方式のビデオのシンタクスを示す。表１における"extention and user data(i)"に"extention data"または"user data"が記録される。

【０１０３】

【表１】

Video Sequence

```
video_sequence ( ) {
        next_start_code ( )
        sequence_header ( )
        if (nextbits ( ) = = extention_start_code) {        ……… MPEG 2  シンタックス
                sequence_extension ( )
                do {
                        extension_and_user_data (0)
                        do {
                                if (next_bits ( ) = = group_start_code) {
                                        group_of_pictures_header ( )
                                        extension_and_user_data (1)
                                }
                                picture_header ( )
                                extensions_and_user_data (2)
                                picture_data ( )
                        } while ((next_bits ( ) = = picture_start_code)||
                                next_bits ( ) = = group_start_code))
                        if (nextbits ( ) ! = sequence_end_code) {
                                sequence_header ( )
                                sequence_extension ( )
                        }
                } while (nextbits ( ) ! = sequence_end_code)
        } else {                                                ……… MPEG1 シンタックス
                do {
                        do {
                                group_of_pictures_header ( )
                                if (next_bits ( ) = = user_data_start_code)
                                        user_data ( )
                                do {
                                    picture_header ( )
                                    if (next_bits ( ) = = user_data_start_code)
                                            user_data ( )
                                        picture_data ( )
                                } while (next_bits ( ) = = picture_start_code)
                        } while (next_bits ( ) = = group_start_code)
                        if (nextbits ( ) ! = sequence_end_code)
                                sequence_header ( )
                } while (nextbits ( ) ! = sequence_end_code)
        }
        sequence_end_code
}
```

【０１０４】表２に表１の"extention and user data (i)"を示す。ここに、"user data start cord"が記載さ

れている場合、次に"user data"が記載されていることを示している。

*【０１０５】

*【表２】

Extension and user data

```
extension_and_user_data (I) {                              No. of bits Mnemonic

    while ((nextbits ( ) = = extension_start_code) ||
                (nextbits ( ) = = user_start_code)) {
        if (nextbits ( ) = = extension_start_code)
                extension_data (i)
        if (nextbits ( ) = = user_start_code)
                user_data ( )
                }
    }

}
```

【０１０６】表３に"user data"を示す。"user data"は、８ビット単位で記録される。例えば、"0000 0000 0000 0000 0000 0001"が発生すると、"user data"が終了※することを意味する。

【０１０７】

【表３】

User data

```
user_data ( ) {                                              No. of bits Mnemonic
      user_data_start_code                                   32  bslbf
      while (nextbits ( ) ! = " 0000 0000 0000 0000 0000 0001") {
              user_data                                      8
      }
      next_start_code ( )
}
```

【０１０８】ＰＳＴフラグは、例えば８ビットのフラグとして""user data"に記憶される。表４にＰＳＴフラグを示す。ここで、例えば、フィルタ１、２、…、Ｎはポストフィルタ２２の各種フィルタを示している。

【０１０９】

【表４】

| ＰＳＴ | フィルタ群 |
|---|---|
| 00000000 | フィルタ 1 |
| 00000001 | フィルタ 2 |
| 00000002 | フィルタ 3 |
| 00000003 | フィルタ 4 |
| ⋮ | ⋮ |
| 11111111 | フィルタ N |

【０１１０】尚、ＰＳＴフラグは、シーケンス、ＧＯＰ、ピクチャヘッダの後に設定可能であるので、次に再設定されるまでその値を用いることが可能であり、即ち、再設定されるまで、同一フィルタが用いられる。

【０１１１】また、ＰＳＴフラグを、シーケンスフラグで設定することも可能であり、この場合の再設定は、シーケンス、ＧＯＰ、ピクチャヘッダの後の"user data"で行うようにしても良い。

【０１１２】記憶媒体３に記憶されたビットストリームは、デコーダ３１で復号化される。このデコーダ３１の構成は、図３に示すように、図１９の従来例で示した復号回路９０と同様に構成されており、ビットストリームが受信バッファ８１を介して復号回路９０の可変長復号化回路８２に入力されると、この可変長復号化回路８２で、可変長符号が解かれる。このとき"user data"に記録されているＰＳＴフラグが復号され、図１に示したポストフィルタ２２に伝送される。その他のデコーダ３１の構成、動作は従来例と同じである。

【０１１３】このように復号化されたＰＳＴフラグによりポストフィルタ２２は、例えば、ポストフィルタ２２の各種フィルタとしてのメディアンフィルタ、ローパスフィルタ等を選択する。尚、メディアンフィルタ、ローパスフィルタはパラメータにより複数種類のフィルタからなるフィルタ群とすることができる。

【０１１４】具体的には、図４に示すように、ポストフィルタ２２は、入力されたＰＳＴフラグに基づいてスイッチ１０１、１０２によりフィルタ１００（１）～１００（Ｎ）を選択し、ビットストリームとしてフレームメ

モリ３４，３５に記憶された色差信号Ｃ及び輝度信号Ｙを、選択したフィルタに出力し、選択されたフィルタにより処理された信号をスイッチ１０３、１０４を介してＤ／Ａ変換器３６、３７に出力する。

【０１１５】次に、ポストフィルタ２２のフィルタの一例としてのメディアンフィルタを説明する。メディアンフィルタは、ブロック歪やモスキートノイズを効果的に除去するフィルタである。図５に示すように、フィールドメモリ群１２０に記憶されている、ある画素の周囲、例えば３×３画素を３×３画素抽出回路１２１で取り出し、並べ変え回路１２２で降べき順に並べ変える。このとき、その中央の値、即ち３×３画素の場合、５番目の値をメディアンと呼ぶが、このメディアン値をＭｅｄｉａｎ検出器１２３で検出し、その画素の値としてＤ／Ａ変換器３６、３７に出力する。メディアンを求めるための画素値はフィルタをかける前の画素値を用いる。

【０１１６】尚、上記のメディアンの算出において、ある画素の周囲３×３画素を用いるとしたが、これに限らず、メディアンを求める画素群はどのように設定しても良い。そして、このメディアンを求める画素群を変えることにより、フィルタの効果を変えることができる。

【０１１７】例えば全ての画素について３×３画素のメディアンをとるメディアンフィルタをかけた場合、ブロック歪等は除去できるが、全体にぼけた画像となる強いフィルタとなる（フィルタ１）。

【０１１８】これに対して、ブロックエッジのみに３×３画素のメディアンをとるメディアンフィルタをかけた場合、ブロック歪を除去すると共に、フィルタ１に比べ高周波成分を維持することができる（フィルタ２）。

【０１１９】また、１次元のメディアンフィルタをかけることができ、この場合フィルタ１、２と比べると、ブロック歪除去の効率は落ちるが、高周波成分を多少維持することができる（フィルタ３）。

【０１２０】このようなフィルタ１、２、３をＰＳＴフラグにより切り換えて最適フィルタを選択する。

【０１２１】このように第１実施例の画像データ符号化・復号化装置によれば、入力されたＰＳＴフラグに基づいて、ポストフィルタ２２でスイッチ１０１、１０２を切り換えることで、最適フィルタを選択することができる。

【０１２２】次に第２実施例ついて説明する。第２実施例は、第１実施例とほとんど同じであり、異なる点はＰＳＴフラグの設定方法が符号化時に発生する各種パラメータに基づいて設定する点であり、その他の構成は第１実施例と同じであるので、異なる構成のみ説明し、同一構成には同じ符号をつけ説明は省略する。

【０１２３】第２実施例のエンコーダ１８におけるＰＳＴフラグ決定方法では、図６に示すように、ポストフィルタ選択回路１４０が、可変長符号化器回路５８に入力される各種パラメータ及びビットカウンタから出力される発生ビット量（符号化パラメータ）に応じて後処理に用いるフィルタを決定する。ポストフィルタ選択回路１４０は、また、使用するポストフィルタを示すＰＳＴフラグを可変長符号化回路５８に出力する。尚、可変長符号化回路５８は、第１実施例と同様にＰＳＴフラグを可変長符号化する。

【０１２４】次に、エンコーダ１８によるＰＳＴフラグの決定方法の１例を説明する。ポストフィルタ２２を特に必要とする場合は、低ビットレートで、かつ符号化効率の悪い場合である。この場合、ブロック歪やモスキートノイズ等が顕著に現れ、画像の劣化が激しくなる。このような画像の劣化を目だたなくなるような後処理が必要となる。一方、高ビットレートで符号化した、符号化効率の良い画像は、復号化されたままで、高画質を維持しているので、過度な後処理を行うことはかえって画質の劣化を引き起こすことになる。

【０１２５】従って、符号化ビットレートが低いほど、ブロック歪等を除去する強いフィルタが必要であり、また符号化効率の悪いシーケンスほど強いフィルタをかける必要がある。

【０１２６】これらを表す符号化パラメータとしては、量子化係数が存在する。この量子化係数は、符号化ビットレートが高くなるほど小さな値をとり、また、符号化効率が良いシーケンスほど小さい値をとる。つまり、この量子化係数の大きさに従って、ＰＳＴフラグを適応的に切り換えれば良いことになる。

【０１２７】量子化係数（quantizer scale code）は、ＭＰＥＧ方式の場合、マクロブロック単位で設定される。マクロブロックシンタクスを表５に示す。

【０１２８】

【表５】

Macroblock layer

```
macroblock() {                                                        No. of bits  Mnemonic
    if(<sequence extension was not present>)
        while(nextbits()=='0000 0001 111')
            macroblock_stuffing                                       11           vlclbf
    while(nextbits()=='0000 0001 000')
        macroblock_escape                                             11           vlclbf
    macroblock_address_increment                                      1-11         vlclbf
    macroblock_modes                                                  ...          ...
    if (macroblock_motion_forward ||
        macroblock_motion_backward) {
        if(picture_structure=="frame") {
            if(frame_pred_frame_dct==0)
                frame_motion_type                                     2            uimsbf
        } else {
            field_motion_type                                         2            uimsbf
        }
    }
    if((picture_structure=="frame")&&
        (frame_pred_frame_dct==0)&&
            (macroblock_intra || macroblock_pattern))
        dct_type                                                      1            uimsbf
    if(macroblock_quant)
        quantizer_scale_code                                          5            uimsbf
    if(macroblock_motion_forward ||
        (macroblock_intra && concealment_motion_vectors))
        forward_motion_vectors()                                      ...          ...
    if(macroblock_motion_backward)
        backward_motion_vectors()                                     ...          ...
    if(macroblock_intra && concealment_motion_vectors)
        marker                                                        1
    if(macroblock_pattern)
        coded_block_pattern()                                         ...          ...
    for(i=0 ; i<block_count ; i++) {
        block(i)                                                      ...          ...
    }
    if(picture_coding_type==4)
        end_of_macroblock                                             1            "1"
}
```

【０１２９】まず、１フレーム符号化した後、１フレーム中の量子化係数の平均値ＭＥＡＮ＿＿Ｑを求める。ＰＳＴフラグが表４のように、ＰＳＴフラグの値が大きいほど強いフィルタに対応している場合、ＭＥＡＮ＿＿Ｑが大きいほど大きなＰＳＴフラグを割り当てる。ＭＥＡＮ＿＿ＱとＰＳＴフラグの関係は、図７（Ａ）に示すように、線形関係であっても、図７（Ｂ）に示す階段状の関係であっても良い（図７（Ｂ）はポストフィルタが頻繁に変化しないような制御方式である）。

【０１３０】尚、ＭＥＡＮ＿＿ＱとＰＳＴフラグの関係は、図７（Ａ）と（Ｂ）のどちらか一方を用いて構成され、符号化装置側と復号化装置側で同一の関係を有するものとする。

【０１３１】具体的には、図８に示すように、ポストフィルタ選択回路１４０では、量子化スケール（量子化係数）が入力されると、平均回路１５０で１フレーム毎にＭＥＡＮ＿＿Ｑが算出される。そして、ＰＳＴ決定回路１５１でＭＥＡＮ＿＿Ｑに基づいてＰＳＴフラグを決定し、可変長符号化回路５８に出力する。その他の構成、作用は第１実施例と同じである。

【０１３２】また、上記の量子化係数を用いる方式の変形として、符号化ビットレートのみを用いる方法があり、この場合、シーケンスヘッダの後でＰＳＴフラグが設定される。

【０１３３】以上説明したように、第２実施例は、第１実施例の効果に加え、ＰＳＴフラグの設定を符号化時に発生する各種パラメータに基づいて行っているので、符号化内容に応じた最適なＰＳＴフラグが設定でき、より最適フィルタを選択することができる。

【０１３４】次に第３実施例ついて説明する。第３実施例は、第２実施例とほとんど同じであり、異なる点はポストフィルタを選択するポストフィルタ選択回路１４０を復号化装置側に設けた点であり、その他の構成は第２実施例と同じであるので、異なる構成のみ説明し、同一構成には同じ符号をつけ説明は省略する。

【０１３５】図９に示すように、第３実施例では、第２実施例で符号化装置１のエンコーダ１８に設けたポストフィルタ選択回路１４０を復号化装置２内に設けて構成している。

【０１３６】第３実施例のデコーダ３１は、図１０に示すように、図１９の従来例で示した復号回路９０と同様に構成されており、ビットストリームが受信バッファ８

１を介して復号回路９０の可変長復号化回路８２に入力されると、この可変長復号化回路８２で、可変長符号が解かれる。このとき符号化パラメータとしての量子化係数が復号化され、ポストフィルタ２２に伝送される。その他の構成、作用及び効果が第２実施例と同じである。

【０１３７】

【発明の効果】以上の説明したように、請求項１に記載の画像処理方法によれば、符号化手段で予測画像信号に基づいて画像信号を符号化する際に画像信号の符号化条件を示す符号化条件フラグを符号化するので、簡単な構成により、画像信号を復号する際に、符号化条件フラグに基づき画像信号を最適に補正することができるという効果がある。

【０１３８】また、請求項１に記載の画像信号符号化装置では、フラグ設定手段で符号化手段が符号化するビットストリームの画像情報の符号化ビットレートに基づき、符号化フラグを設定するので、画像信号をより最適に補正することができるという効果がある。

【０１３９】請求項４に記載の画像信号復号化装置によれば、画像補正手段で画像信号の符号化条件を示す符号化条件フラグに基づいて、復号化された画像信号を補正することで、簡単な構成により、画像信号を復号する際に、符号化条件フラグに基づき画像信号を最適に補正することができるという効果がある。

【図面の簡単な説明】

【図１】本発明の画像データ符号化・復号化装置の第１実施例の構成を示すブロック図である。

【図２】図１のエンコーダ１８の構成を示すブロック図である。

【図３】図１のデコーダ３１としての復号回路９０の構成を示すブロック図である。

【図４】図１のポストフィルタ２２の構成を示すブロック図である。

【図５】図４のポストフィルタ２２のフィルタ例としてのメディアンフィルタの構成を示すブロック図である。

【図６】本発明の第２実施例のエンコーダ１８の構成を示すブロック図である。

【図７】図６のポストフィルタ選択回路１４０の作用を説明する説明図である。

【図８】図６のポストフィルタ選択回路１４０の構成を示すブロック図である。

【図９】本発明の画像データ符号化・復号化装置の第３実施例の構成を示すブロック図である。

【図１０】図９のデコーダ３１としての復号回路９０の構成を示すブロック図である。

【図１１】高能率符号化の原理を説明する図である。

【図１２】画像データを圧縮する場合におけるピクチャのタイプを説明する図である。

【図１３】動画像信号を符号化する原理を説明する図である。

【図１４】画像信号符号化装置と復号化装置の構成例を示すブロック図である。

【図１５】図１４におけるフォーマット変換回路１７のフォーマット変換の動作を説明する図である。

【図１６】図１４におけるエンコーダ１８の構成例を示すブロック図である。

【図１７】図１６の予測モード切り替え回路５２の動作を説明する図である。

【図１８】図１６のＤＣＴモード切り替え回路５５の動作を説明する図である。

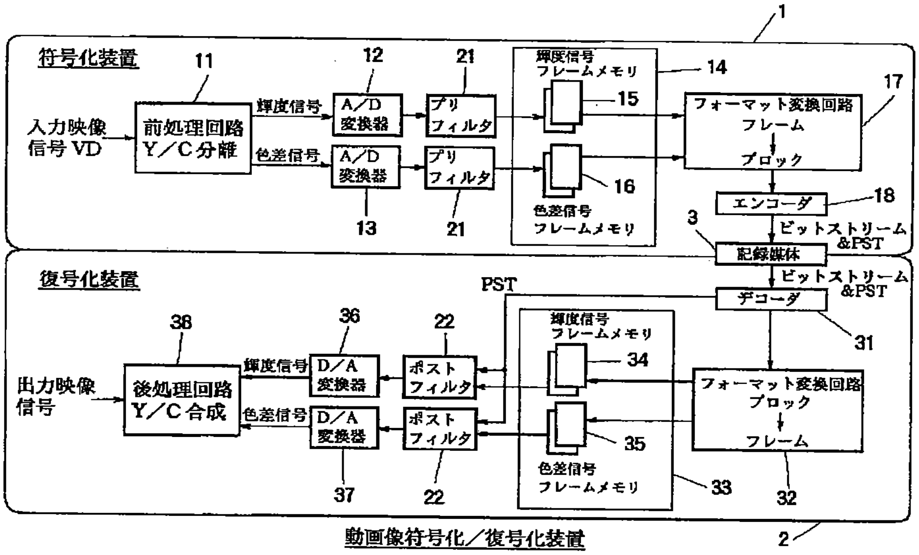
【図１９】図１４のデコーダ３１の１例である復号回路９０の構成例を示すブロック図である。

【符号の説明】

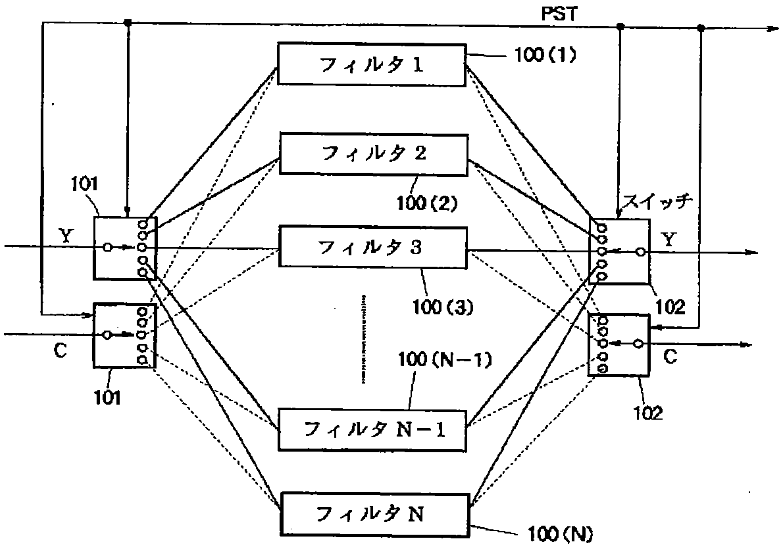
| | |
|---|---|
| １ | 符号化装置 |
| ２ | 復号化装置 |
| ３ | 記録媒体 |
| １２，１３ | Ａ／Ｄ変換器 |
| １４ | フレームメモリ |
| １５ | 輝度信号フレームメモリ |
| １６ | 色差信号フレームメモリ |
| １７ | フォーマット変換回路 |
| １８ | エンコーダ |
| ２１ | プリフィルタ |
| ２２ | ポストフィルタ |
| ３１ | デコーダ |
| ３２ | フォーマット変換回路 |
| ３３ | フレームメモリ |
| ３４ | 輝度信号フレームメモリ |
| ３５ | 色差信号フレームメモリ |
| ３６，３７ | Ｄ／Ａ変換器 |
| ４９ | ピクチャ判定回路 |
| ５０ | 動きベクトル検出回路 |
| ５１ | フレームメモリ |
| ５２ | 予測モード切り替え回路 |
| ５３ | 演算部 |
| ５４ | 予測判定回路 |
| ５５ | ＤＣＴモード切り替え回路 |
| ５６ | ＤＣＴ回路 |
| ５７ | 量子化回路 |
| ５８ | 可変長符号化回路 |
| ５９ | 送信バッファ |
| ６０ | 逆量子化回路 |
| ６１ | ＩＤＣＴ回路 |
| ６３ | 演算器 |
| ６４ | フレームメモリ |
| ６５ | 動き補償回路 |
| ８１ | 受信バッファ |
| ８２ | 可変長復号化回路 |
| ８３ | 逆量子化回路 |
| ８４ | ＩＤＣＴ回路 |

８６　演算器
８７　フレームメモリ
８８　動き補償回路
１００（1）～１００（N）　フィルタ１～フィルタＮ
１０１、１０２　スイッチ
１２１　３×３画素抽出回路
１２２　並べ変え回路
１２３　Ｍｅｄｉａｎ検出回路
１４０　ポストフィルタ検出回路
１５０　平均回路
１５１　ＰＳＴ決定回路

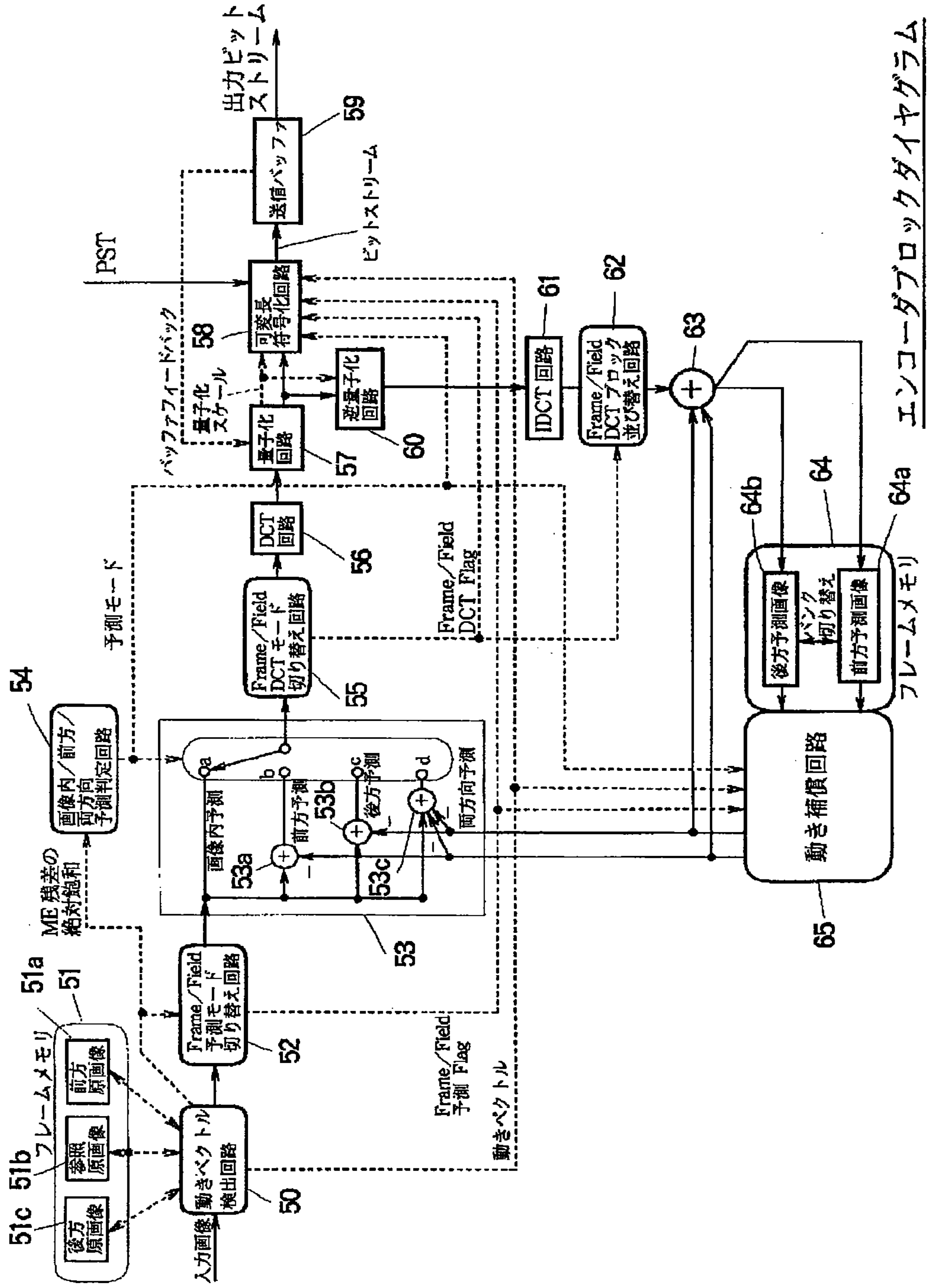
【図１】



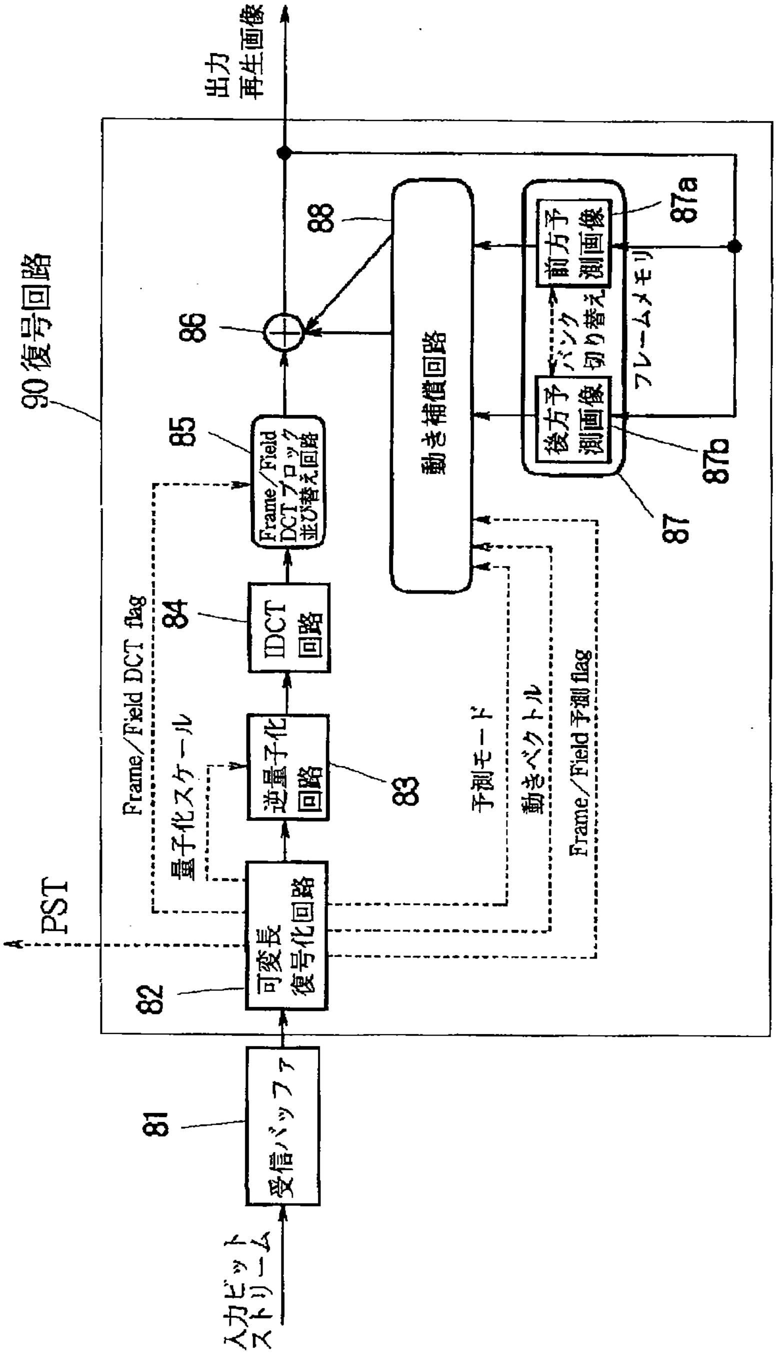
【図４】



【図２】

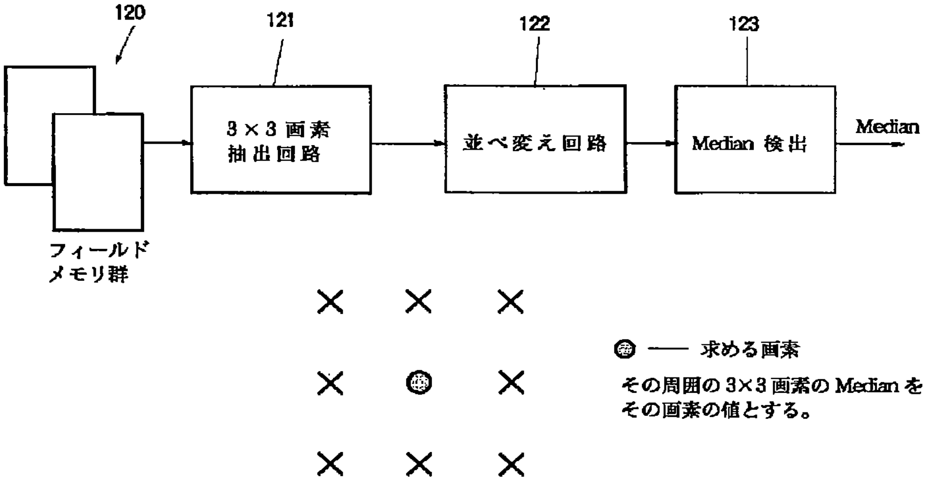

入力画像
動きベクトル検出回路
50
後方原画像
参照原画像
前方原画像
フレームメモリ
51
51a
51b
51c
Frame／Field予測モード切り替え回路
52
Frame／Field予測 Flag
動きベクトル
ME残差の絶対値和
画像内／前方／両方向予測判定回路
54
予測モード
53
53a
53b
53c
画像内予測
前方予測
後方予測
両方向予測
a
b
c
d
Frame／Field DCTモード切り替え回路
55
DCT回路
56
Frame／Field DCT Flag
量子化回路
57
量子化スケール
逆量子化回路
60
可変長符号化回路
58
PST
ビットストリーム
送信バッファ
59
出力ビットストリーム
バッファフィードバック
IDCT回路
61
Frame／Field DCTブロック並び替え回路
62
63
後方予測画像
前方予測画像
バンク切り替え
フレームメモリ
64
64a
64b
動き補償回路
65
エンコーダブロックダイヤグラム

【図3】

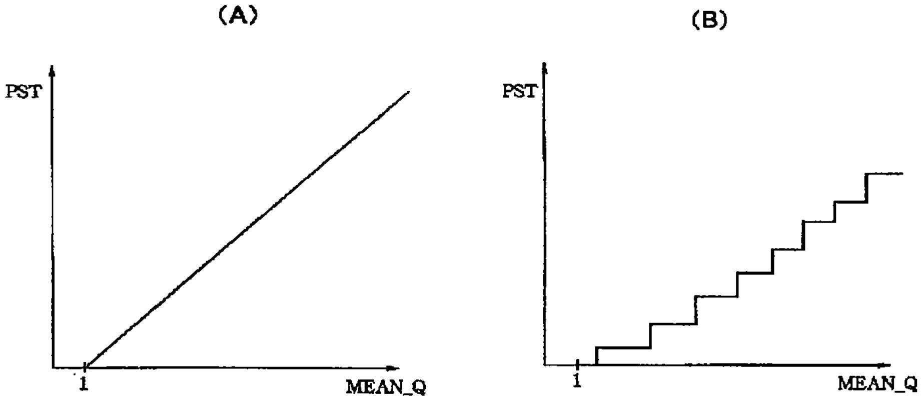


デコーダブロックダイヤグラム

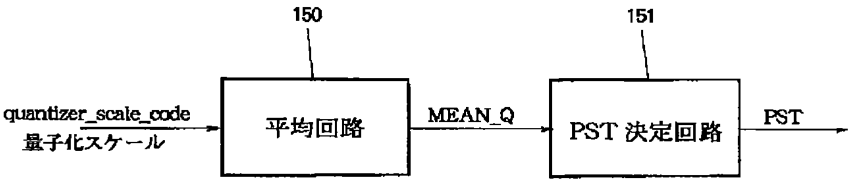
【図5】


120
121
122
123
3×3画素
抽出回路
並べ変え回路
Median 検出
Median
フィールド
メモリ群
● —— 求める画素
その周囲の3×3画素の Median を
その画素の値とする。

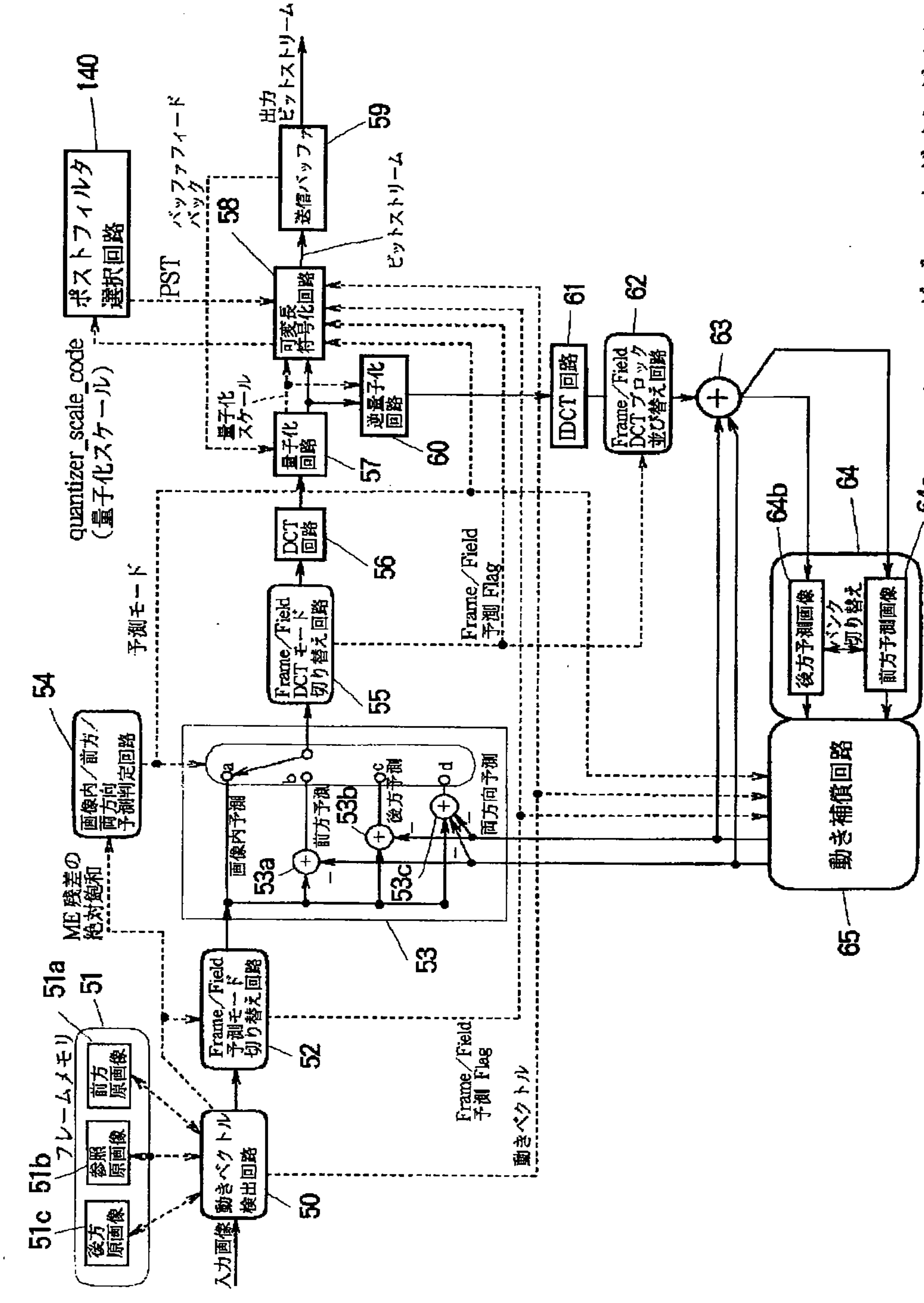
【図7】


(A)
(B)
PST
1
MEAN_Q
PST
1
MEAN_Q

【図8】

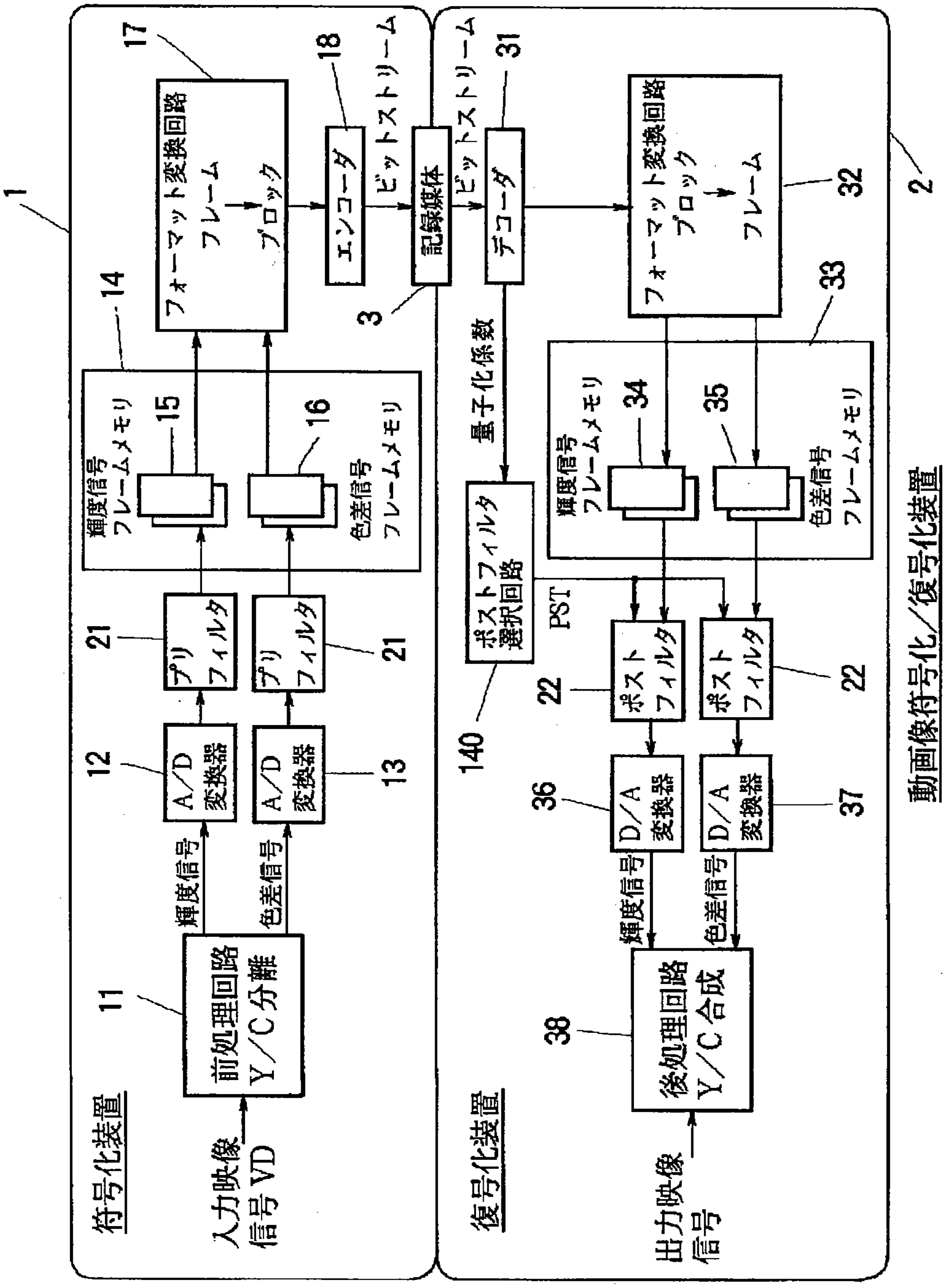

150
151
quantizer_scale_code
量子化スケール
平均回路
MEAN_Q
PST 決定回路
PST

【図６】

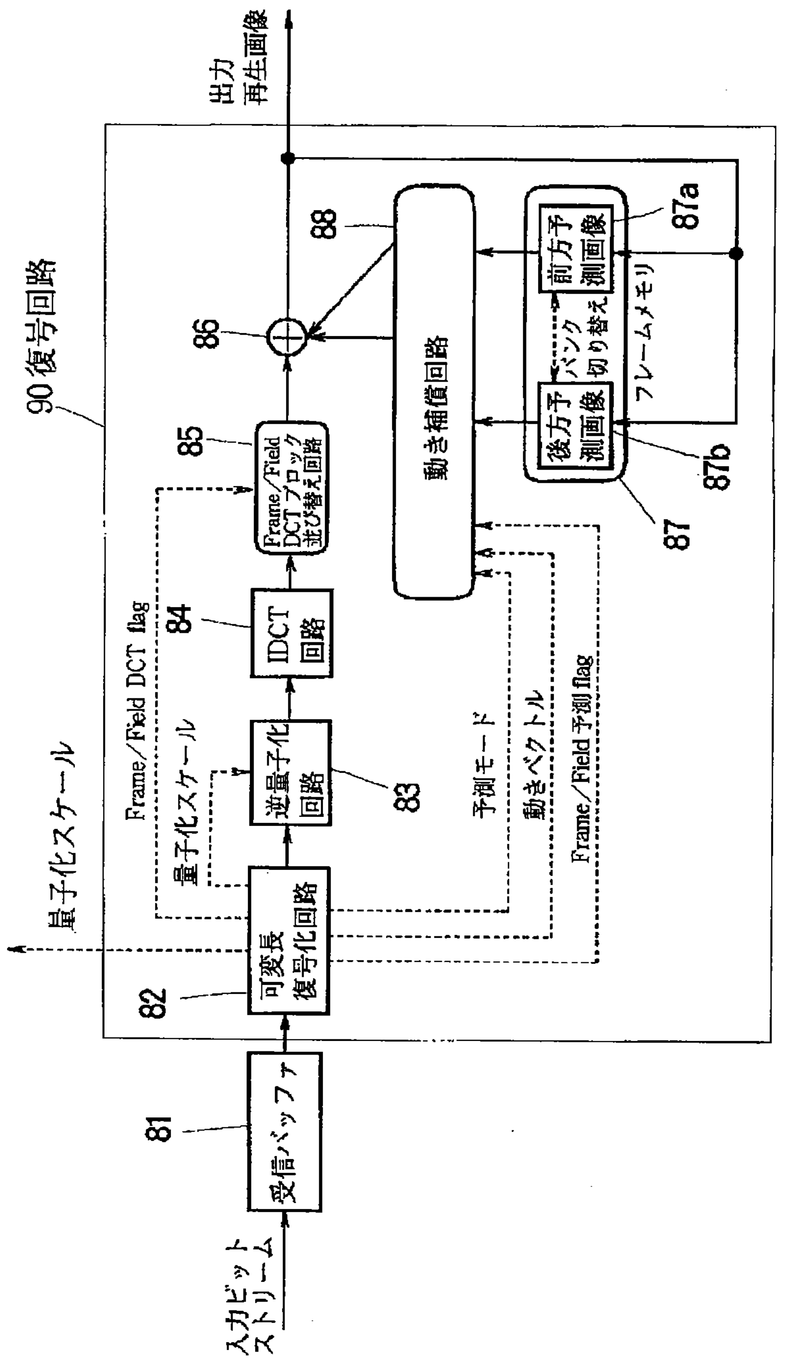


エンコーダブロックダイヤグラム

【図9】

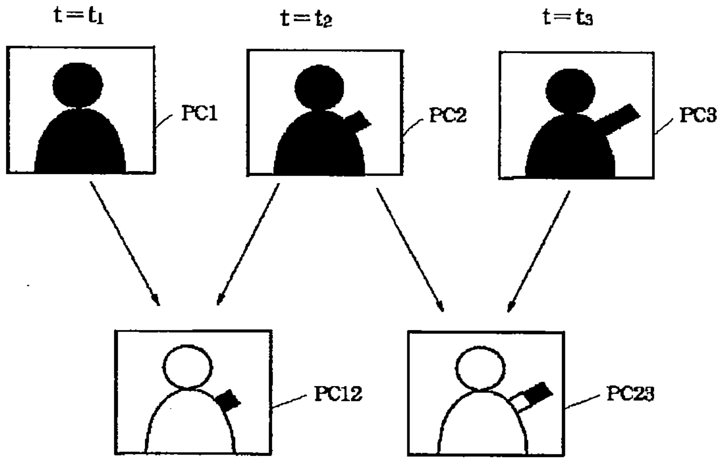

動画像符号化／復号化装置
符号化装置
入力映像信号VD
前処理回路 Y／C分離
輝度信号
色差信号
A／D変換器
プリフィルタ
輝度信号フレームメモリ
色差信号フレームメモリ
フォーマット変換回路 フレーム → ブロック
エンコーダ
ビットストリーム
記録媒体
復号化装置
デコーダ
量子化係数
ポストフィルタ選択回路
PST
フォーマット変換回路 ブロック → フレーム
ポストフィルタ
D／A変換器
後処理回路 Y／C合成
出力映像信号
1
2
3
11
12
13
14
15
16
17
18
21
22
31
32
33
34
35
36
37
38
140

【図１０】



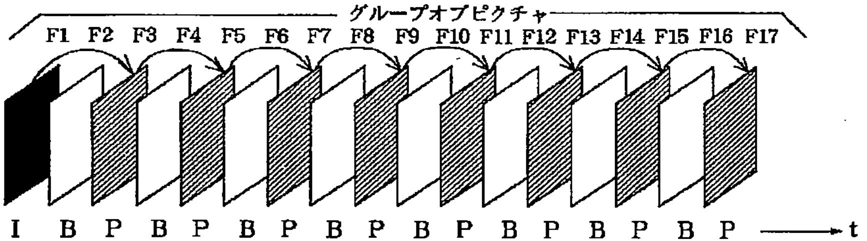
デコーダブロックダイヤグラム

【図１１】

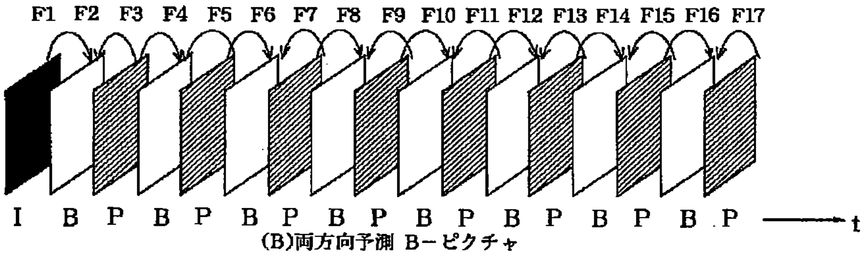


高能率符号化

【図１２】


グループオブピクチャ
F1 F2 F3 F4 F5 F6 F7 F8 F9 F10 F11 F12 F13 F14 F15 F16 F17
I B P B P B P B P B P B P B P B P
t

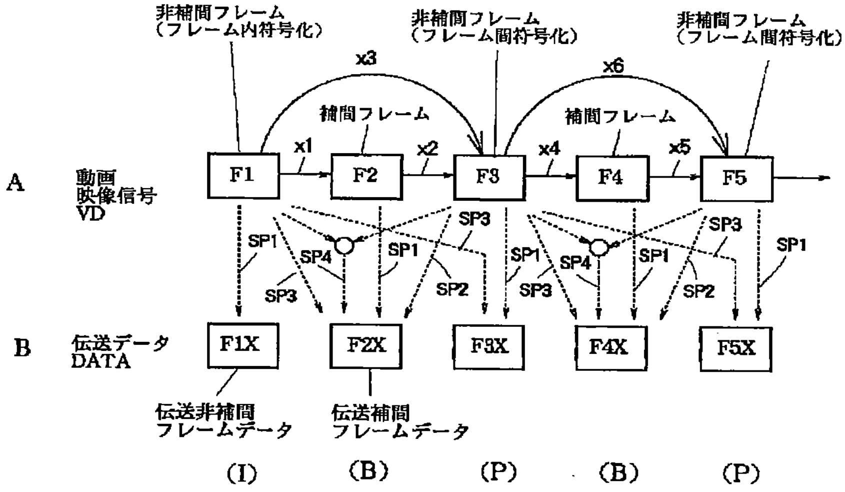
(A)前方向予測 P−ピクチャ


F1 F2 F3 F4 F5 F6 F7 F8 F9 F10 F11 F12 F13 F14 F15 F16 F17
I B P B P B P B P B P B P B P B P
t

(B)両方向予測 B−ピクチャ

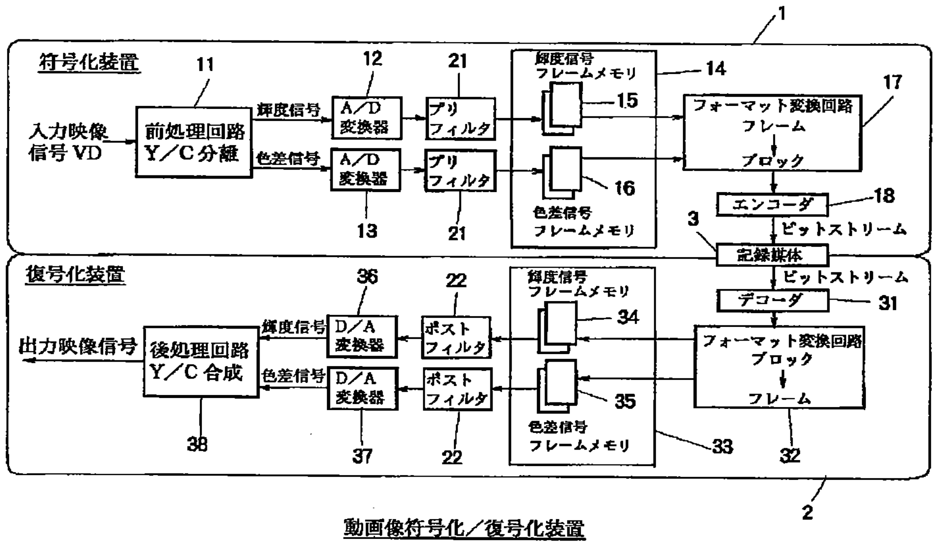
ピクチャタイプ I, P, B−picture

【図１３】



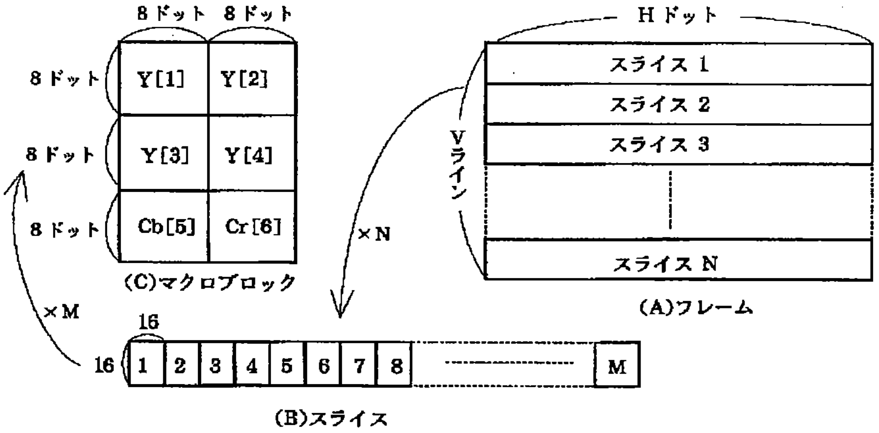
動画信号符号化方法の原理

【図１４】



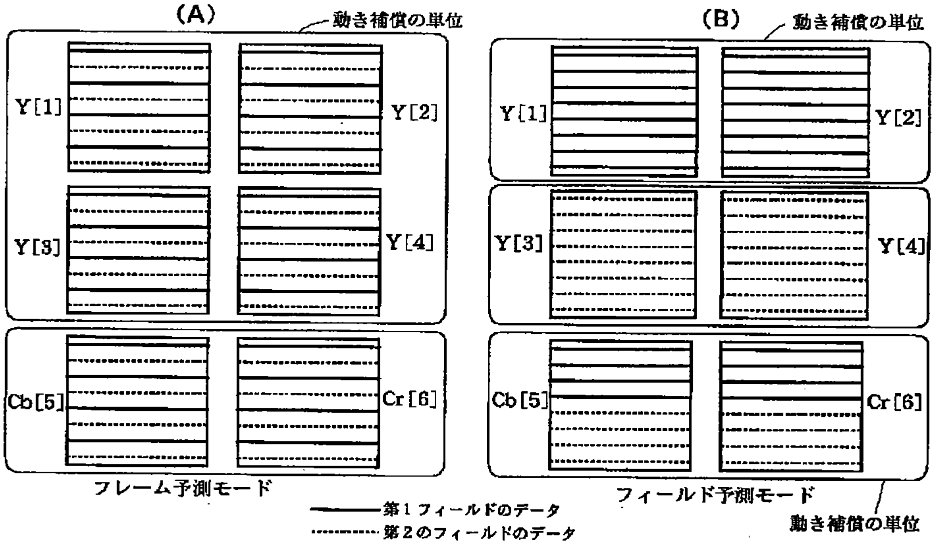
動画像符号化／復号化装置

【図１５】



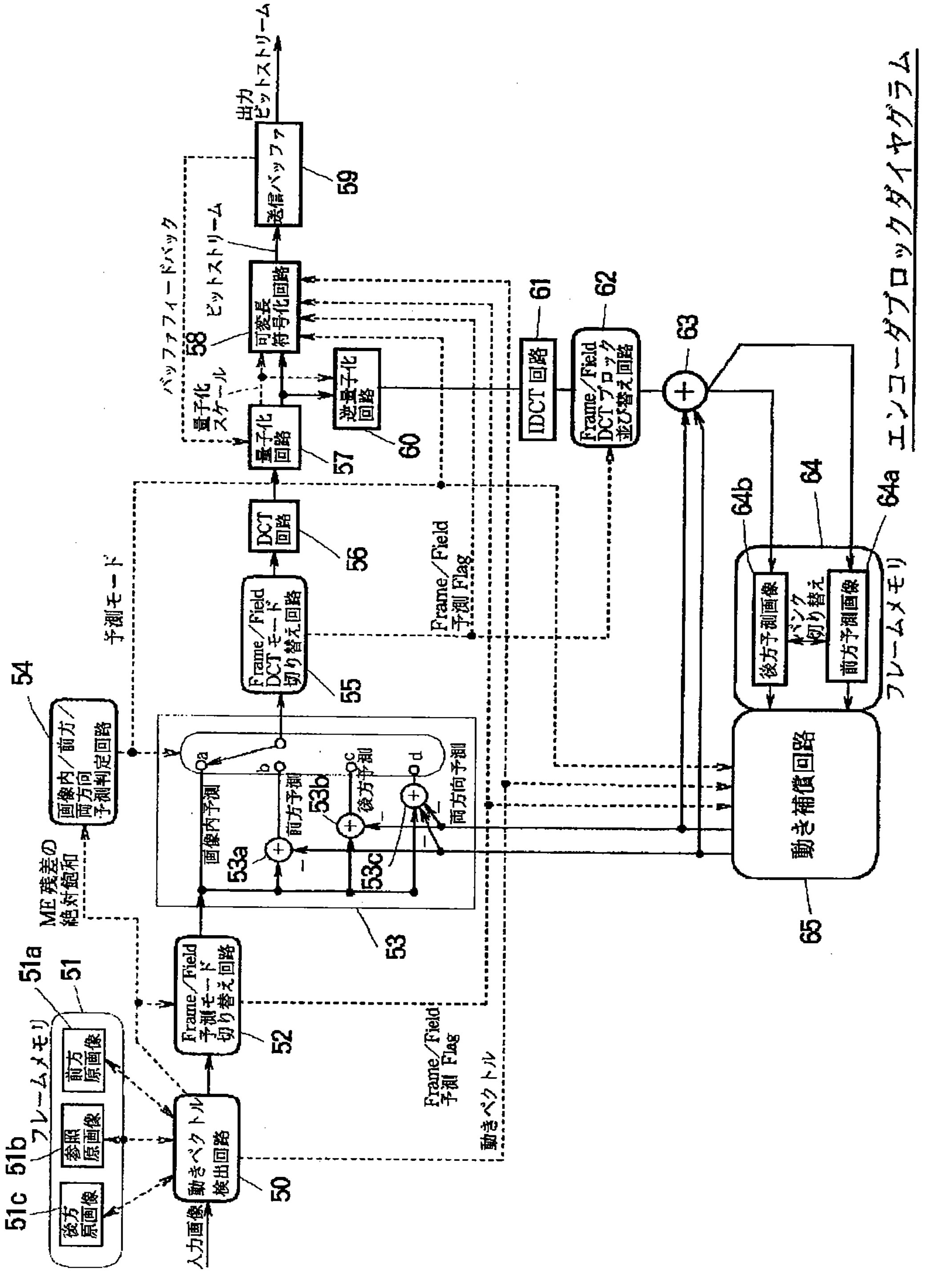
画像データの構造

【図１７】



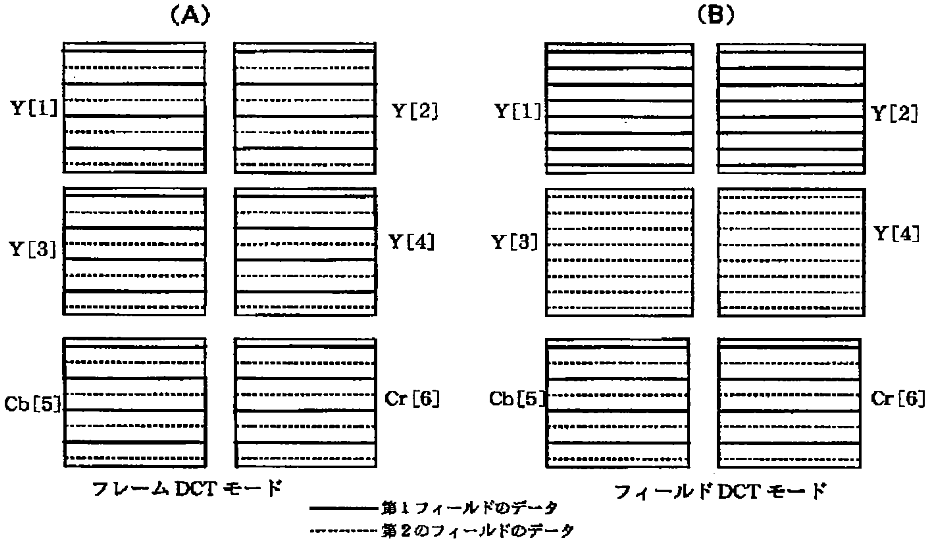
フレーム／フィールド予測モード

【図１６】



エンコーダブロックダイヤグラム

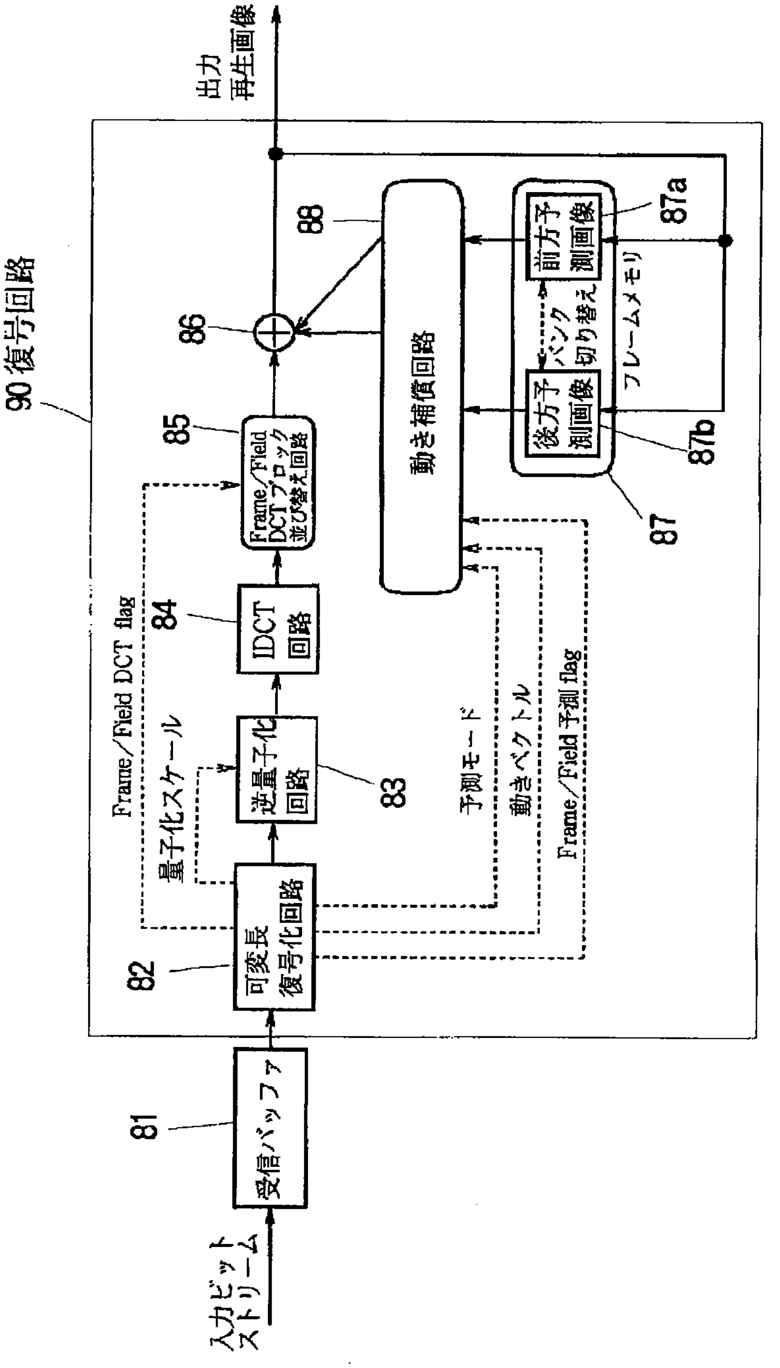
【図１８】



フレームDCTモード　　フィールドDCTモード

フレーム／フィールドDCTモード

【図１９】



デコーダブロックダイヤグラム